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A sigma-delta architecture for recording of peripheral neural signals in prosthetic applications.

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***Abstract*— A recording module for peripheral neural signals is presented. The proposed device, based on a sigma-delta architecture, is made up of two main parts: an analog module as front-end stage for neural signal acquisition, pre-filtering and sigma-delta modulation and a digital unit for sigma delta decimation and system configuration. The analog module provides a gain of $200V/V$ in a $800Hz - 8kHz$ frequency range, while the sigma-delta converter grants a $9bit$ resolution and a good noise rejection thanks to the 32^{nd} order decimator IIR filter. Behavioural and transistor-level simulation results confirm that the system is capable of recording neural signals in the order of magnitude of tens of μV eliminating the huge low frequency noise due to electromyographic interferences.**

I. INTRODUCTION

Brain Machine Interfaces (BMIs) have recently drawn a great deal of attention by scientists. In fact, BMIs have a wide range of biomedical applications, as in treatments of diseases affecting the nervous system [1], [2], [3], as well as in neuro-prosthetics [4], [5]. This work deals with the latter field: the system is aimed at recording the signals extracted from the peripheral nervous system of an amputee patient and at exploiting them to drive a robotic hand. This approach is highly innovative and promises several advantages with respect to the traditional Electromyographic (EMG) prostheses. First because, by using the same signals used to control the biological limb, the patient gets potentially closer to feeling the prosthetic arm as a natural extension of his/her body. Moreover the neural approach allows for a more selective and versatile solution in view of sensory feedback restoring [6]. One of the key problems in the development of such a system is represented by neural signal acquisition. Peripheral neural signals show amplitudes in the order of tens of μV [7], [8] and are subject to noise due to contractions of the muscles near the electrodes (EMG interferences). Such noise is in the order of magnitude of mV and can thus mask the neural signal. Furthermore, Power Spectral Densities (PSDs) of the interferences and of the useful signal are very close to each other and partially overlap [9], [10]. A front-end amplification/filtering stage is then mandatory in order to boost the weak neural signal and to filter out the huge EMG components. Many papers concerning neural interfaces have been presented in literature, but the majority of them are focused on the Central Neural System (CNS) [7], [11].

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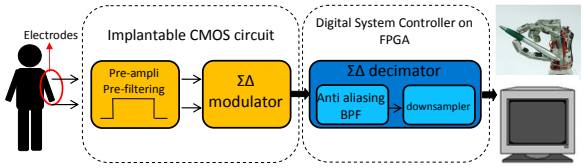


Fig. 1. System architecture

The most pursued approach in works devoted to Peripheral Neural System (PNS) recording is oriented to a fully analog implementation based on multi-stage high selective filters [12], [13], [14] followed by standard, Nyquist-rate, Analog to Digital Converters (ADC). An alternative approach is based on oversampling converters. In [15] a first order sigma delta converter has been designed, reaching a 8 bit resolution with a 40 oversampling ratio over a $6.25kHz$ frequency. A second order sigma delta modulator that exploits a new superinverter amplifier has been proposed in [16] and allows to reach a 11 bit resolution considering a $8kHz$ bandwidth. Following the latter approach, we propose a system based on a sigma-delta architecture which combines high resolution and high integration altogether with the possibility of easily decoupling the sensitive and potentially implantable analog module and the robust, external digital module. Sigma-delta oversampling converters are particularly suited for low bandwidth applications since they are capable of increasing the achieved resolution by increasing the sampling frequencies. Moreover, they shift the design complexity from the analog to the digital domain. In this way, it is possible to integrate on an implantable chip only a limited number of simple, low-power, low-noise analog components. Such components include a pre-filtering stage and the sigma-delta modulator, made-up of integrators and a 1-bit quantizer. The output signal is represented by the 1-bit output of the quantizer thus requirements for the communication channel are less stringent, as well. The complex digital unit that finalizes the A/D conversion and provides the highly selective filter needed to eliminate the EMG interferences, can thus be accommodated on an external digital module such as a Field-Programmable Gate Array (FPGA) or an Application Specific Integrated Circuit (ASIC).

II. SYSTEM ARCHITECTURE

The block diagram in Fig. 1 shows the system architecture of the proposed neural recording module which is composed of two main components: the analog front/end and the digital processing unit. The signal is, thus, filtered and amplified

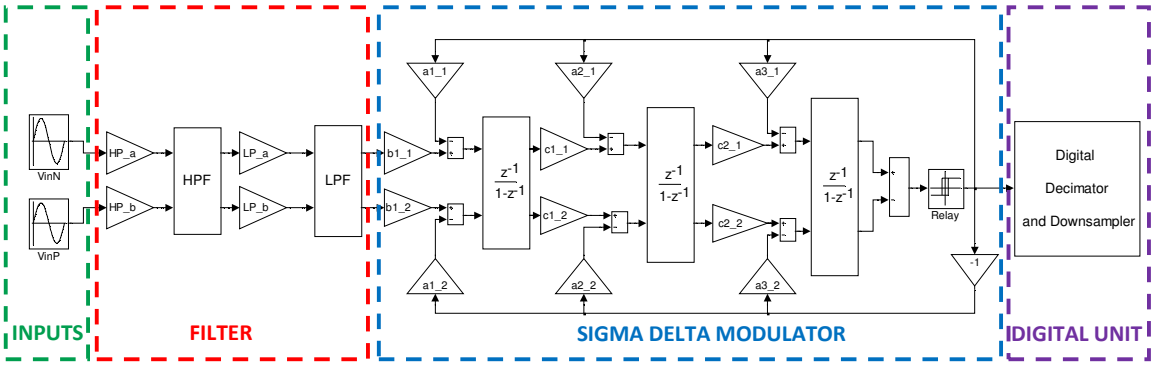


Fig. 2. Behavioral Simulink model

by the Pre-Filtering/Pre-amplifier block as close as possible to the recording site. In this way, the noise due to cables and connection paths can be avoided. The conditioned signal is then converted into a 1-bit digital stream by the sigma-delta modulator and sent to the digital module for decimation and further processing. One of such signal's streams is needed for each input channel if the device is connected to a multichannel electrode. The digital module is hosted on an external board; it implements the decimation block of the sigma-delta converter altogether with the highly selective bandpass filter. The digital module is also responsible of management of the communication between the artificial limb and the implanted electrodes. The hardware digital unit has been implemented and tested on a Xilinx Virtex 5 LX330 FPGA to be hosted on the robotic limb.

A. Design and modelling of the analog module

The analog part of the circuit is composed by the pre-amplifier/pre-filtering block and by a third order sigma-delta modulator (Fig. 2). The Band-Pass Filter (BPF) was realized cascading a High-Pass Filter (HPF) with a Low-Pass Filter (LPF). The frequency response specifications require a bandwidth between $800Hz$ and $8kHz$ and a gain of $200V/V$. The required gain is determined by the need to maximize the amplification at neural signal frequencies avoiding the risk of amplifier saturation due to EMG interferences. Once that the useful signal has been properly amplified it is possible to convert it in the digital domain. With this purpose, a third order switched-capacitor, sigma-delta modulator in a Cascade of Integrators with FeedBack (CIFB) configuration was designed. Preliminary tests were performed using a behavioural model (shown in Fig. 2) in Simulink environment and, only once that the specifications were satisfied, the circuit was implemented at transistor level in a $0.35\mu m$ CMOS technology process from Austriamicrosystems (AMS).

The Simulink model has great advantages in terms of simulation time saving and it allows the modelling of noise sources and operational amplifier (OpAmp) non-idealities, thus ensuring a good agreement with transistor level simulations. The sigma-delta behavioural model is a modification of what presented in [17] and [18] that take into consideration saturation, slew rate, finite gain and bandwidth limitations. KT/C noise, thermal noise of the amplifier, switches non-idealities and clock jitter effects have also been included. The original models were adapted to accurately model the switched-capacitors, fully-differential architecture of the implemented circuit. Component's mismatch effects were also modeled by generating the filter coefficients as capacitor ratios whose values have been extracted randomly from a normal distribution within a 6σ range around the nominal value. Non-idealities of the switches take into account the use of transmission gates (pair of NMOS-PMOS switches) and the clock jitter has been modified in order to consider the differential path of the fully-differential architecture. The complete model, including all non-idealities and the digital decimation described later is shown in Fig. 3.

The HPF and LPF transfer functions in the frequency domain (Eq. 1 and Eq. 2) can be easily determined once that cut-off frequencies have been defined ($\tau_{hp} = 1/f_{hp}$ and $\tau_{lp} = 1/f_{lp}$).

$$TF_{hp}(s) = \frac{\tau_{hp}s}{\tau_{hp}s+1} \quad (1) \qquad TF_{lp}(s) = \frac{1}{\tau_{lp}s+1} \quad (2)$$

The equivalent expression for the discrete time domain can be obtained using the bilinear transform (or Tustin's Method) based on the equivalence of Eq. 3

$$s \approx \frac{2}{T} \times \frac{z-1}{z+1} \quad (3)$$

The resulting transfer function are reported in Eq. 4 and Eq. 5

$$TF_{hp}(z) = \frac{2\tau_{hp} - 2\tau_{hp}z^{-1}}{(2\tau_{hp}+T) - (2\tau_{hp}-T)z^{-1}} \quad (4)$$

$$TF_{lp}(z) = \frac{T + Tz^{-1}}{(2\tau_{lp}+T) - (2\tau_{lp}-T)z^{-1}} \quad (5)$$

where T is the sample period and τ is the filter time constant. The closed loop transfer function is then expressed by Eq. 6, where $TF(z)$ is the filter transfer function of Eq. 1 or Eq. 2 and A is the finite gain of the open loop amplifier.

$$TF_{CL}(z) = \frac{TF(z)}{1 + \frac{TF(z)}{A}} \quad (6)$$

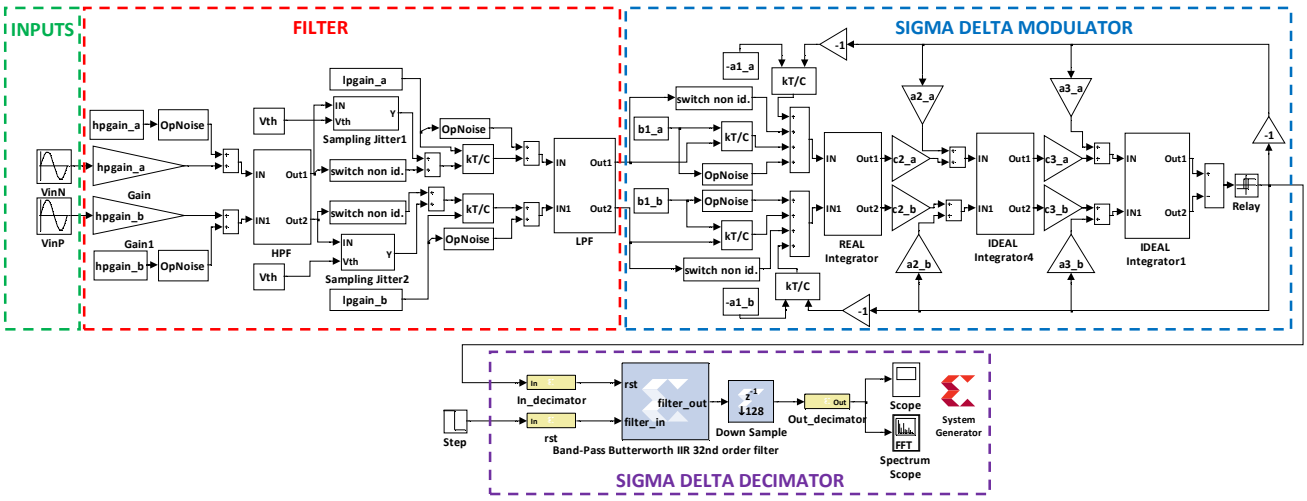


Fig. 3. Behavioural Simulink model including non-idealities and digital module

TABLE I
SIGMA DELTA MODULATOR: COEFFICIENTS

Coefficient	Value	Coefficient	Value
a_1	0.05	b_1	0.05
a_2	0.3	c_1	1
a_3	0.8	c_2	1

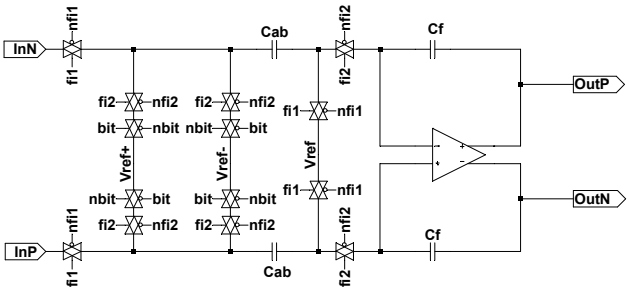


Fig. 5. Sigma-delta modulator: first integrator schematic

The coefficients (summarized in in Table I) of the sigma-delta modulator were chosen using the Schreier Toolbox [19] with a 18-bits target resolution. The oversampling ratio that allows to reach this target resolution is $OSR = 128$ that, considering a signal bandwidth of $8kHZ$ results in a sampling frequency $f_s = 2.048MHz$.

For what concerns the transistor implementation, the pre-filter stage was implemented as shown in Fig. 4 while the integrators of the sigma-delta modulator as shown in Fig. 5.

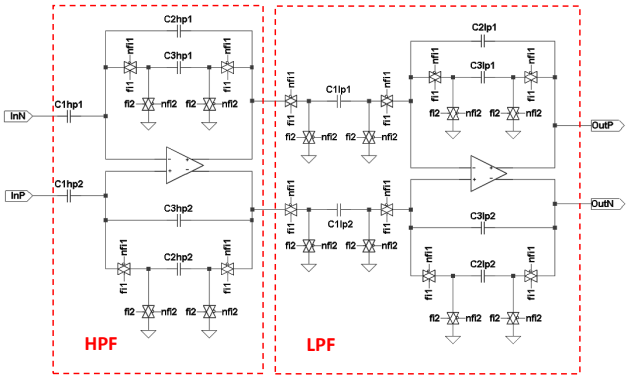


Fig. 4. Band-Pass filter

B. Design and realization of the digital module

The main task of the digital block is to elaborate the oversampled 1-bit signal provided by the analog modulator. In order to remove the EMG noise at low frequencies and the quantization noise pushed at high frequencies by the analog modulator, it is necessary to use a high-order bandpass anti-aliasing filter as the first decimator stage, before the down-sampler. The filter works at the same sampling frequency of the modulator which is equal to $2.048MHz$, with a 128 oversampling ratio with respect to the Nyquist frequency ($16kHz$ in our case). For these reasons, we decided to design a band-pass filter characterized by a selective frequency response in order to clean up the 1-bit $800Hz - 8kHz$ oversampled signal from the EMG and quantization noise. Good performances have been obtained using a Butterworth IIR filter with a $3dB$ attenuation at $800Hz$ and $8kHz$ cutoff frequencies, as first stage of the decimator. IIR filters have been chosen for their high efficiency compared to that offered by FIR filters, in fact, they require less memory and fewer multipliers-accumulators. The main drawbacks are due to the instability problems, but they occur less likely using, as in this case, high order filter designed by cascading second-order systems [20]. Using MATLAB tools, a 32^{nd} order Butterworth IIR BPF has been created with the required frequency response and simulated in Simulink environment.

TABLE II

DIGITAL DESIGN PARAMETERS

Response Type	Band-Pass Filter
Design Method	IIR Butterworth
Filter Arithmetic	Fixed-Point
Passband	0.8 - 8 KHz
Input Sampling Frequency	2.048 MHz
Order	32
Coefficient Word Length	32 bit
Input Word Length	32 bit
Input Fraction Length	20 bit
Output Word Length	32 bit
Rounding Mode	Floor
Overflow Mode	Wrap

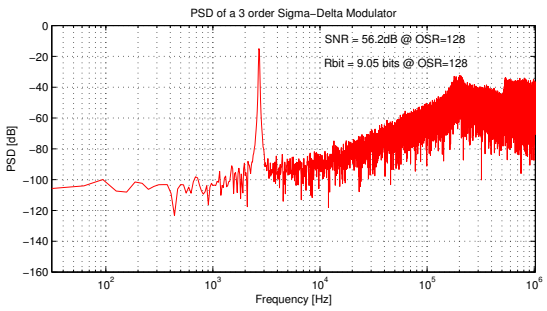


Fig. 6. Sigma delta modulator: Power spectral density of the complete real model

A downsampler has been cascaded to the IIR filter; it is characterized by a simple HDL implementation, corresponding to a hardware module that picks up one sample every R which represents the oversampling factor equal to 128 in our case. After verifying the correct operation of the IIR filter on Simulink using a double-precision floating-point representation of internal signals, we evaluated the same functionality in the case of fixed-point implementation. Values reported in Table II represent a good design parameter choice.

The possibility of using a multistage Cascaded Integrator-Comb filter (CIC filter) [21], that is characterized by the higher power-and-area efficiency, has also been investigated. Anyhow, such solution was discarded since the correspondent frequency response does not respect the design constraints. In fact, CICs have a low-pass behaviour, so it would still be necessary the use of a high-selective IIR or FIR high-pass filter working at the oversampling clock frequency in order to cut the EMG noise at low frequencies. Moreover, the use a 3rd order analog modulator requires the implementation of a CIC filter with a minimum of 4 sections [22]. In order to obtain a higher attenuation between the passband and the stopband, the filter order should be further increased resulting in a large number of bits for the internal delay registers to avoid overflows.

The decimation filter and downsampler were coded in HDL and mapped on a FPGA. We adopted a specific solution for the IIR filter which has the second direct form using 16 second-order sections and a CSD representation for the 2's complement internal signals [23]. A hardware-software co-simulation using Xilinx System Generator (Fig. 3) was setup. In particular, the co-simulation allows to simulate the Simulink model of the analog module (including all non-idealities) and to send the results directly to the HDL implementation of the designed digital decimation filter mapped on FPGA. In this way, the software blocks generate the oversampled 1-bit stream that is set as input of a specific pin of the FPGA. The $2.048MHz$ sampling frequency was generated using a clock enable that delays significant edges of the board clock signal in order to handle the synchronization of the digital decimation filter with the output signal coming from the software analog blocks. The designed decimation filter was tested on a Xilinx Virtex 5 LX330 but the hardware implementation can be mapped on a Spartan 3E XC3S1600E, characterized by a lower integration capacity, with a slices utilization equal to 100%.

III. SIMULATION RESULTS

The PSD of the output signal for a full-scale sinusoidal input allows to compute the Effective Number of Bits (ENOB) achievable by the converter. Considering only the sigma-delta modulator, without taking into account non-idealities effects and with an input at $2.7kHz$ of a $0.5V$ amplitude, the modulator grants to achieve a $SNR = 98dB$ corresponding to an ENOB of $16bit$.

PSD results obtained simulating all the recording chain (filter + modulator), including also all the noise sources, show a deep degradation in terms of resolution, leading to a $SNR = 56dB$ corresponding to a $9bit$ converter resolution (Fig. 6). The plot was obtained using an input with an amplitude of $2mV$ at $2.7kHz$. It should be clear that this is a worst case, in which noise has been extra-estimated, while in real implementation we expect to have better noise performances.

Fig. 7 depicts the system response in terms of SNR for increasing input amplitudes. As expected, the SNR increases for increasing input amplitudes and starts to degrade when a $2mV$ input amplitude is reached. This value corresponds to a modulator input of $0.5V$, i.e. $V_{ref}/2$. The sigma-delta

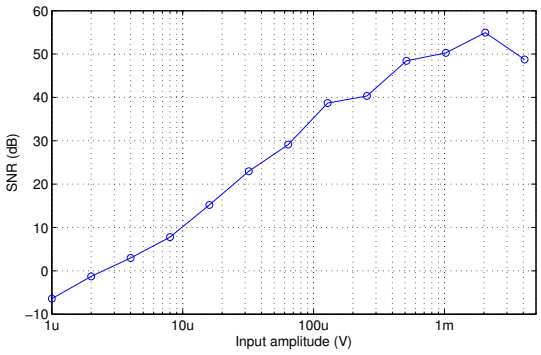
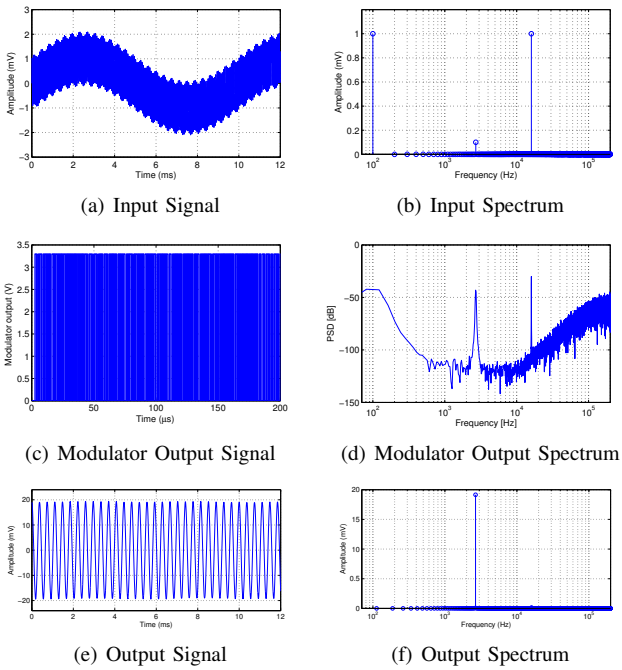


Fig. 7. Signal to Noise Ration variations with different signal amplitudes



(a) Input Signal (b) Input Spectrum

(c) Modulator Output Signal (d) Modulator Output Spectrum

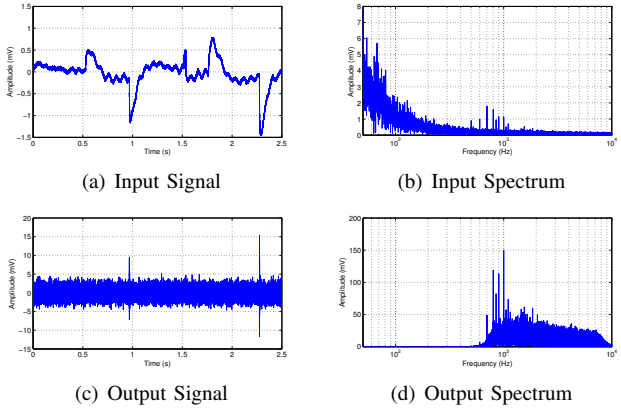
(e) Output Signal (f) Output Spectrum

Fig. 8. Recording chain response to an input composed by the sum if three sines at $100Hz$, $2.7kHz$ and $16kHz$

modulator performances drop drastically [19] because of saturation. It can be observed that the minimum detectable signal (corresponding to $SNR = 0dB$) is equal to $2\mu V$.

Transistor level design was validated by simulating the whole recording chain with an input given by the sum of 3 sine waves at 3 different frequencies. A $100\mu V$ signal at $2.7kHz$ has been used to emulate the neural signal, while two components with an amplitude of $1mV$ at $100Hz$ and $16kHz$ have been used to model out-of-band interferences. In particular, the low-frequency sine wave represents a realistic EMG signal. The input signal is shown in Fig. 8(a) and Fig. 8(b). The signal has been pre-filtered and pre-amplified by the analog block before being converted in a $1-bit$ stream by the sigma delta modulator. The resulting signal is shown in Fig. 8(c) and its PSD can be observed in Fig. 8(d). The 3 components are still detectable and, as expected, the $2.7kHz$ component has been amplified more than the two out-of-band signals. The noise shaping effect due to the delta delta modulator is also evident. In order to remove the unwanted components, the signal has been decimated with a 32^{nd} order IIR Butterworth filter implemented in a Virtex 5 LX330 FPGA. The results in the time and frequency domain are reported in Fig. 8(e) and Fig. 8(f); it is evident how the unwanted components are completely filtered out and only the in-band frequency, amplified by the $45.5dB$ filter gain, is allowed to pass. The results obtained with transistor level simulation are then exactly what expected, confirming the high reliability of the developed behavioural model.

Once that the proper behaviour of the Simulink model has been confirmed comparing short-simulation time results with those achieved in Cadence environment, longer simulations can be reliably run using the more lean and flexible Simulink model.



(a) Input Signal (b) Input Spectrum

(c) Output Signal (d) Output Spectrum

Fig. 9. Sigma Delta modulator: pre-recorded neural signal processing

In order to evaluate the system capability to work with real neural signals, the whole system has been tested with a pre-recorded neural signal extracted in clinical trials from the PNS of a rabbit subjected to cutaneous afferent stimulation at $50Hz$ and $100Hz$. The signal was filtered and modulated by the Simulink model of the analog module and the resulting stream of bits was fed to the IIR decimator filter mapped on the Xilinx Virtex 5 LX330 FPGA. The input pattern, represented in Fig. 9(a), corresponds to 2.5 seconds of recording. The input signal is affected by EMG and ECG interferences with a very large amplitude (in the millivolts range) and a spectrum (Fig. 9(b)) concentrated below $300Hz$. Such interferences completely mask the underlying neural content. Fig. 9(c) displays the input-referred output signal and Fig. 9(d) its power spectral density: the low-frequency interferences are completely removed and the weak neural signal is now amplified and visible, as well as its frequency signature. We also performed some tests by processing a part of the track recorded in absence of external stimulation and, as expected, no evidence of neural spikes was detected and only the underlying noise was visible at the system output.

IV. CONCLUSION

A neural recording interface for peripheral nervous system based on a sigma-delta architecture was conceived, designed and simulated. The proposed device is composed by an analog front-end unit (pre-filter and modulator) modelled at behavioural (Simulink) and transistor level and by a digital module hosted on a Xilinx Virtex 5 LX330 FPGA. The analog module amplifies and filters the weak neural signal as close as possible to the recording site and converts it in a digital bit stream by means of a third order single loop sigma-delta modulator. The digital unit provides sigma-delta decimation and downsampling as well as configuration and control the analog part. The converter, including noise effects, exhibits a $SNR = 56.2dB$ corresponding to $9-bit$ resolution allowing the recording module to detect signals in the order of magnitude of tens of microvolt.

V. ACKNOWLEDGMENTS

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