A High-efficiency Cascade Multilevel Class-D Amplifier with Sliding Mode Control

ZHANG Ying CAI Ling MENG Qing-De
Naval Academy of Armament
Naval Academy of Armament, NAA
Beijing, China
zyxgyxdd1008@sina.com

LI Yao-hua
Institute of Electrical Engineering
Chinese Academic of Science, CAS
Beijing, China
yhli@mail.iee.ac.cn

Abstract — **The article presents a new switch-mode power amplifier based on a cascade multilevel topology. The amplifier adopts phase-shifted PWM technology and enjoys a switching frequency, which is 2N times of that of a single unit. It has a small total output voltage ripple and only requires a small filter to suppress the switching frequency harmonics. The article lays emphasis on the design of the sliding mode control and deducts the parameters, and then develops a 2kW cascade multilevel class-D power amplifier adopting sliding mode control. The research results show that this kind of amplifier significantly increases the system bandwidth, provides the system with fast following performance and stability, high efficiency, and low THD value of output signals, no matter the system is under resistive load or bridge rectifier load.**

Keywords — **class-D power amplifier, multilevel control, phase-shifted PWM control, sliding mode control.**

I. INTRODUCTION

Power amplifiers are used to generate high current and high voltage in industrial measurement, test and machining. The common power amplifiers are divided into class A, AB, B, C, D, with decreasing fidelity and increasing efficiency. Currently power amplifiers are mostly class A and B power amplifiers, which have good dynamic performance, wide bandwidth and good linearity. However, they also have large power consumption, low efficiency, and high cost. With the development of semi-conducting devices, the switch-mode class-D power amplifier replaces the linear power amplifier in many fields. Class-D power amplifier has low power consumption and high efficiency of normally over 90%. However, its fidelity is not as good as that of class A and B power amplifier and its output voltage has relatively low bandwidth. So researchers suggest that multilevel converter should be adopted to improve the output quality of class-D power amplifier[1-3]. The multilevel power conversion technology[4~5] is to synthesize several level steps into a ladder wave which is close to a sine output voltage. The more level steps are synthesized, the higher the resolution is, and the closer the output voltage waveform is to the sine wave.

Currently multilevel converters mainly have three topologies: ① Diode-clamped converter.② Capacitor-clamped converter. ③ Cascade converter. With the same switching devices and the same switching frequency and level, cascade converter has the following features: fewer devices; lower output harmonics; easy to realize modular design, assembly and debugging. In the utilization of multilevel technology, in order to further improve system performance, Paper[6] adopts closed-loop control of voltage to control the trigger signals, which is good for the control of resistive load, but not ideal for the control of non-linear and non-resistive loads. Sliding mode control[7] is a control method applied since 1990s. It has successful applications in AC servo motor control[8]-[9], PWM converter control[10~11] and DC/DC converter control[12]. The application of this method in class-D power amplifier based on multilevel topology is a question worthy of deep study. The article designs a cascade class-D power amplifier adopting a multilevel topology composed of four full-bridge units. Its trigger control adopts phase-shifted PWM, forming a sliding mode control to ensure the following quality of output signals. As the output LC lowpass filter is included in the loop, this control method can compensate the attenuation caused by the LC lowpass filter, thus ensuring the bandwidth and quality of output signals.

II. BASIC TOPOLOGY OF THE SYSTEM

Fig.1 is the topology of a multilevel class-D power amplifier adopting four cascade full-bridge units with the same DC voltage. The output filter is an inductance-capacitance type and the phase-shifted PWM modulation is adopted to provide trigger signals for the power switches.

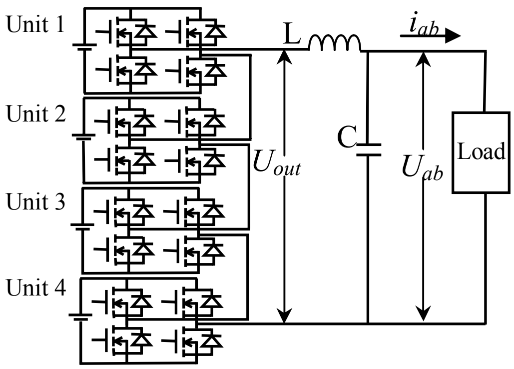


Fig1. The topology of a cascade multilevel class-D power amplifier.

The N cascade full-bridge units have the same structure with the same DC voltage (E_d). The frequency of the triangular carrier waves is f_s=25kHz and the amplitude is V_{tr}. There is a phase shift ($\theta=1/2Nf_s=5\mu s$) between the triangular carrier waves of two neighboring units. The PWM signal of each unit is generated through the comparison of positive and negative signals of the triangular carrier waves and output reference waves (the frequency of the modulated wave is f_0 and the amplitude is Q_{km}). The degree of modulation is $M=Q_{km}/V_{tr}$ and the amplitudes of the fundamental waves and harmonics are respectively[13]:

a. The fundamental signal output:

$$k = f_0 ,\ C_1 = NME_d \tag{1}$$

b. Carrier wave harmonic:

$$k = 2mNf_s (m = 1,2,3\ldots), C_k = 0 \tag{2}$$

c. Side band harmonic:

When $k = 2mNf_s + nf_0, m = 1,2,\ldots, n = \pm1,\pm2,\ldots$,

$$C_k = \frac{E_d}{m} J_n(2mNM)\sin[(2mN+n)\frac{\pi}{2}] \tag{3}$$

Wherein: $J_n(\cdot)$ is n-order Bessel function.

Table I is a harmonic analysis table of a 9 level PWM output signal in different degrees of modulation.

III. FEATURE ANALYSIS OF THE SLIDING MODE CONTROL

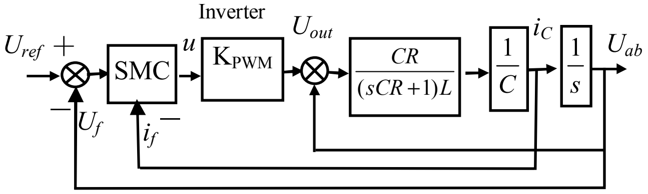


Fig 2. Block diagram of sliding mode controllers of a cascade multilevel class-D power amplifier.

Fig 2. is the block diagram of the sliding mode control. Set the sliding mode controller's output signal is u, then the cascade multilevel class-D power amplifier' state equation is:

$$\begin{bmatrix} \frac{di_C}{dt} \\ \frac{dU_{out}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{1}{CR} & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} i_C \\ U_{out} \end{bmatrix} + \begin{bmatrix} \frac{K_{PWM}}{L} \\ 0 \end{bmatrix} u \tag{4}$$

Set U_{ref} is the voltage reference input signal, so the states variable is:

$$\begin{cases} x_1 = U_{ref} - U_{out} \\ x_1' = U_{ref}' - U_{out}' = x_2 \end{cases} \tag{5}$$

We can obtain:

TABLE I A HARMONIC ANALYSIS TABLE OF A 9 LEVEL PWM OUTPUT SIGNAL IN DIFFERENT DEGREES OF MODULATION

($f_s = 25kHz, f_0 = 2kHz, N = 4$)

F M	Harmonic Degrees								
	m=0	m=1 (100)				m=2 (200)			
		n=±1	n=±3	n=±5	n=±7	n=±1	N=±3	n=±5	n=±7
M=0.25	0.25	0.0165	0.1075	0.033	0.0038	0.0147	0.0182	0.0116	0.02
M=0.5	0.5	0.0587	0.0728	0.0464	0.0801	0.0056	0.0027	0.0036	0.0114
M=0.75	0.75	0.0559	0.0488	0.0184	0.0426	0.0096	0.0101	0.0101	0.0081
M=1.0	1	0.0226	0.011	0.0144	0.0456	0.0017	0.0006	0.0016	0.0048

$$\begin{cases} U_{out} = U_{ref} - x_1 \\ x_1' = U_{ref}' - \frac{1}{C} i_C = x_2 \end{cases} \tag{6}$$

Therefore:

$$x_2' = -\frac{1}{CL}x_1 - \frac{1}{CR}x_2 - \frac{K_{PWM}}{CL}u + (U_{ref}'' + \frac{1}{CR}U_{ref}' + \frac{1}{CL}U_{ref}) \tag{7}$$

Set $a_0 = \frac{1}{CL}$, $a_1 = \frac{1}{CR}$, $b = \frac{K_{PWM}}{CL}$, reference input signal is: $m = \frac{1}{CL}U_{ref} + \frac{1}{CR}U_{ref}' + U_{ref}''$.

Then "(5)" is:

$$\begin{cases} x_1' = x_2 \\ x_2' = -a_0 x_1 - a_1 x_2 - bu + m \end{cases} \tag{8}$$

Set the sliding surface:

$$s = c_0 x_1 + x_2 \qquad c_0 > 0 \tag{9}$$

Select the system state feedback control law:

$$u = \varphi_1 x_1 + \varphi_2 x_2 + f\,\mathrm{sgn}(s) \tag{10}$$

Where:

$$\varphi_i = \begin{cases} \alpha_i & x_i s > 0 \\ \beta_i & x_i s < 0 \end{cases} \quad i = 1,2 \tag{11}$$

f is a constant of gain, sgn is a sign function.

Therefore:

$$\begin{aligned} s' &= c_0 x_1' + x_2' \\ &= -a_0 x_1 + (c_0 - a_1)x_2 - bu + m \end{aligned} \tag{12}$$

Then:

$$\begin{aligned} ss' &= -a_0 x_1 s + (c_0 - a_1) x_2 s - bus + m \\ &= (-b\varphi_1 - a_0) x_1 s + (c_0 - a_1 - b\varphi_2) x_2 s + (m - f\,\mathrm{sgn}(s)) s \end{aligned} \tag{13}$$

The necessary condition for the existence of conventional sliding modes is:

$$\lim_{s \to 0} s \cdot s' \leq 0 \tag{14}$$

So we can get the value of α, β [14]:

(1) If $x_1 s > 0$, $\varphi_1 = \alpha_1$, $-a_0 - b\alpha_1 < 0$, Then:

$$\alpha_1 > -\frac{a_0}{b} = -\frac{1}{K_{PWM}} \tag{15}$$

(2) If $x_1 s < 0$, $\varphi_1 = \beta_1$, $-a_0 - b\beta_1 > 0$, Then:

$$\beta_1 < -\frac{a_0}{b} = -\frac{1}{K_{PWM}} \tag{16}$$

(3) If $x_2 s > 0$, $\varphi_2 = \alpha_2$, $c_0 - a_1 - b\alpha_2 < 0$, Then:

$$\alpha_2 > \frac{c_0 - a_1}{b} = \frac{c_0 CL}{K_{PWM}} - \frac{L}{RK_{PWM}} \tag{17}$$

(4) If $x_2 s < 0$, $\varphi_2 = \beta_2$, $c_0 - a_1 - b\beta_2 > 0$, Then:

$$\beta_2 > \frac{c_0 - a_1}{b} = \frac{c_0 CL}{K_{PWM}} - \frac{L}{RK_{PWM}} \tag{18}$$

(5) If $s > 0$, $m - bf < 0$,Then:

$$f > \frac{m}{b} = \frac{1}{K_{PWM}} U_{ref} + \frac{L}{RK_{PWM}} U'_{ref} + \frac{CL}{K_{PWM}} U''_{ref} \tag{19}$$

(6) If $s < 0$, $m + bf > 0$,Then:

$$f > -\frac{m}{b} = -\frac{1}{K_{PWM}} U_{ref} - \frac{L}{RK_{PWM}} U'_{ref} - \frac{CL}{K_{PWM}} U''_{ref} \tag{20}$$

So we can get the value of φ_1, φ_2 :

$$\begin{cases} \alpha_1 > -\dfrac{1}{K_{PWM}} & x_1 s > 0 \\ \beta_1 < -\dfrac{1}{K_{PWM}} & x_1 s < 0 \\ \alpha_2 > \dfrac{c_0 CL}{K_{PWM}} - \dfrac{L}{RK_{PWM}} & x_2 s > 0 \\ \beta_2 < \dfrac{c_0 CL}{K_{PWM}} - \dfrac{L}{RK_{PWM}} & x_2 s < 0 \\ f > \left| \dfrac{1}{K_{PWM}} U_{ref} + \dfrac{L}{RK_{PWM}} U'_{ref} + \dfrac{CL}{K_{PWM}} U''_{ref} \right| & s > 0 \text{或} s < 0 \end{cases} \tag{21}$$

If the parameters are selected according to “(21)”, the necessary condition for the existence of conventional sliding modes can always be satisfied, and the sliding mode movement is insured to stabilization. So the dynamic characteristic of the system is independent of system’s and filter’s parameters, but nearly correlate with the sliding mode’s coefficient c_0 and φ_1, φ_2, f.

Set N=4, R=20Ω, f_0=2kHz, f_s=25kHz, E_d=50V, V_{tr}=15V, Set filter parameters: L=0.2mH, C=0.25μF, Then: K_{PWM}=13.3. We can obtain:

$$\begin{aligned} f &> \left| \frac{1}{K_{PWM}} U_{ref} + \frac{L}{RK_{PWM}} U'_{ref} + \frac{CL}{K_{PWM}} U''_{ref} \right| \\ &> 0.075 U_{ref} + 7.5 \times 10^{-7} U'_{ref} + 3.75 \times 10^{-12} U''_{ref} \\ &> 0.075 U_{ref} \end{aligned} \tag{22}$$

Set $k > 0.075$, Then:

$$f = kU_{ref} \tag{23}$$

So the controller’s output u is:

$$u(t) = \varphi_1 \int x_1 dt + \varphi_2 x_1 + \int f dt \tag{24}$$

Where f is a function of U_{ref}, which is independent of the error and can be treat as a compensative value. So the controller’s output u is similar as the general PI controller, but its integral coefficient φ_1 and proportion coefficient φ_2 is changing. So this controller has stronger ability of resisting disturbs.

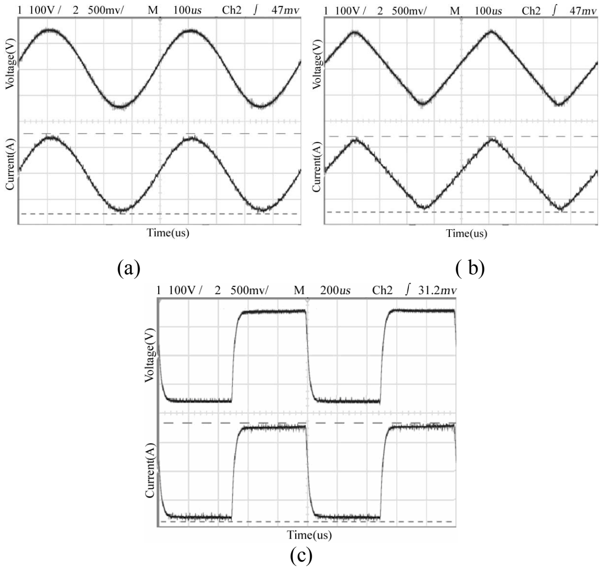
Ⅳ. EXPERIMENT RESULTS AND ANALYSIS

According to the above analysis results, a 2kW cascade multilevel class-D power amplifier is developed with the following parameters as shown in table II.

Fig 3. is the output current and voltage waveforms with resistive load using SMC controller when different input signals are given. From the figure we can see that the proposed amplifier has good following performance.

TABLE II THE PARAMETERS OF THE CLASS-D POWER AMPLIFIER

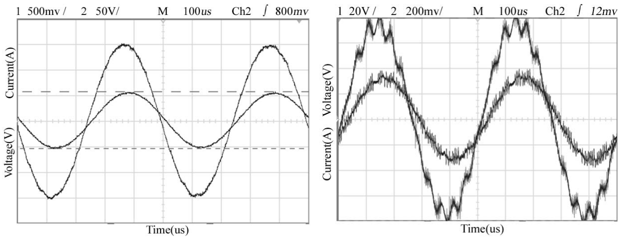
Output voltage	U=±200V
Output current	i_0≈±10A
Rating load	R=20Ω
Switching frequency	f_s=25kHz
Number of units	N=4
DC voltage	E_d=50V
Modulated wave frequency	f_0=2kHz
Output filter	L=0.2mH,C=0.25μF
Cut-off frequency of the filter	f_d=22.5kHz
Sliding mode controller	c_0=20, α_1=1, β_1=-1, α_2=1.5, β_2=-0.5



(a) (b)

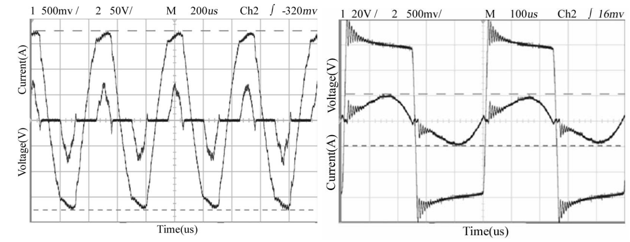
(c)

Fig 3. The Output Voltage and Current waveform with resistive load using SMC control.(a)-(c) Upper traces: U_{ab} (100V/div); lower traces: i_{ab} (5A/div).(a) 2kHz sine wave response, 100us/div. (b) 2kHz triangular wave response, 100us/div. (c) 1kHz square wave response, 200us/div.



(a) (b)

Fig 4. The output current and voltage waveform of the class-D power amplifier with inductive load (R=20Ω, L=0.292mH) using SMC and PI control when the input is 2kHz sine wave. (a) SMC control, 100us/div, traces 1: i_{ab} (5A/div); traces 2: U_{ab} (50V/div). (b) PI control, 100us/div, and traces 1: U_{ab} (20V/div); traces 2: i_{ab} (2A/div).



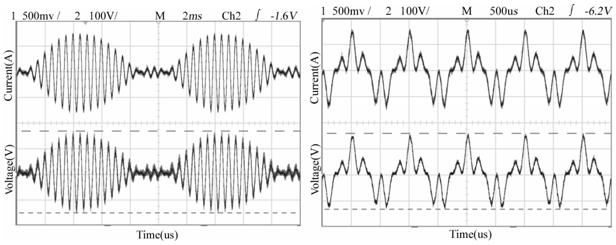
(a) (b)

Fig 5. The output current and voltage waveform of the class-D power amplifier with full-bridge rectifier load using SMC and PI control when the input is 2kHz sine wave. (a) SMC control, 200us/div, traces 1: i_{ab} (5A/div); traces 2: U_{ab} (50V/div). (b) PI control, 100us/div, traces 1: U_{ab} (20V/div); traces 2: i_{ab} (5A/div).

Fig 4. is the output current and voltage waveform of the class-D power amplifier with inductive load (R=20Ω, L=0.292mH) using SMC and PI control when the input is 2kHz sine wave. From the figure we can see that the amplifier's output current and voltage waveform under SMC controller is better than the waveform under PI controller.

Fig 5. is the output current and voltage waveform of the class-D power amplifier with full-bridge rectifier load using SMC and PI control when the input is 2kHz sine wave. From the figure we can see that the amplifier's output current and voltage waveform under SMC controller is better than the waveform under PI controller.

Fig 6. is the output voltage and current waveform of the class-D power amplifier with resistive load when different frequencies are input. From the figure we can see that the amplifier has good following control performance.



(a) (b)

Fig 6. The Output Voltage and Current waveform of the class-D power amplifier with resistive load when different frequencies signals are input. (a)-(b) Upper traces: i_{ab} (5A/div), lower traces: U_{ab} (100V/div). (a) SMC control, 2ms/div. (b) SMC control, 500us/div.

Fig 7. is the amplitude and phase frequency characteristics of the class-D amplifier adopting sliding mode control and PI dual closed-loop control. From the figure we can see that, compared with PI dual closed-loop control, the system bandwidth of sliding mode control increases from 5.25kHz to 10.5kHz.

Fig 8. is the efficiency characteristics of the proposed amplifier. From the figure we can see that its efficiency is above 93%.

Fig 9. is the THD curve of output voltage with resistive load when different input signals are given. From the figure, we can see that the output voltage THD is less than 2% when the input signal frequency is less than 10kHz.

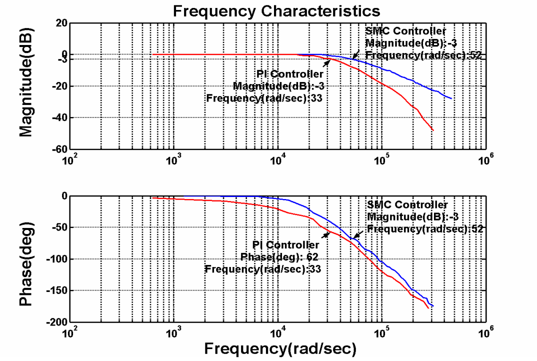


Fig 7. Amplitude and phase frequency Characteristics.

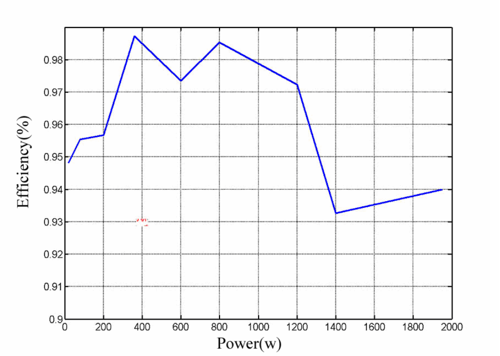


Fig 8. Efficiency characteristics of the amplifier

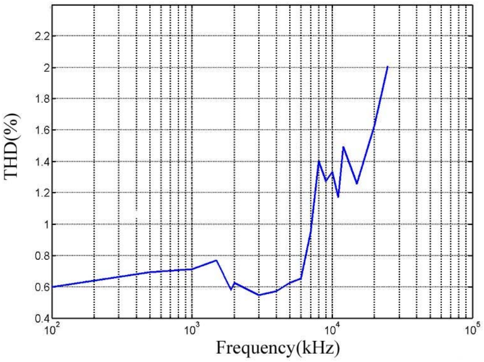


Fig 9. The THD curve of output voltage with resistive load when different input signals are given

V. CONCLUSIONS

The article lays emphasis on the research of a multilevel class-D power amplifier adopting sliding mode control, deducts the parameters and develops a 2kW cascade multilevel class-D power amplifier adopting sliding mode control. The research results show that this kind of amplifier has significantly improved system bandwidth, which provides the system with good following performance and stability under resistive load or bridge rectifier load, high efficiency and low output signal THD value.

REFERENCES

[1] H. Ertl, J.W.Kolar and F. C. Zach, " Basic considerations and topologies of switched-mode assisted linear power amplifiers," IEEE Trans. Ind. Electron, vol. 44, pp.116-122, Feb 1997.

[2] G.R.Stanley and K.M.Bradshaw, "Precision DC-to-AC power conversion by optimization of the output current waveform-The half-bridge revisited," In: Proceeding of the 28th IEEE power Electronics Specialists conference, St.Louis, Missouri, USA, vol. 35, pp. 993-999, Feb 1997.

[3] Isao Takahashi, Kazuki Iways, "High Efficiency Low Harmonic Distortion Switching Type Power Amplifier Using Multilevel Inverter ," Power conversion conference, Osaka, Janpan, pp.353-358, 2002.

[4] BO Bao-zhongm, SU Yan-min, MA Xue-liang. "Application of Sliding-Mode control scheme in three-level converter," Journal of circuits and systems Proceeding of the CESS, vol. 22, pp.89-92, Feb 2002.

[5] WU Hong-yang, HE Xiang-ning. "Relationspbip between multilevel carrier-based PWM and SVPWM and its applications," vol. 22, pp. 10-15, May 2002.

[6] Hans Ertl, Johann W.kolar, "Analysis of a Multilevel Multicell Switch-Mode Power Amplifier Employing the Flying-Battery Concept," IEEE Transactions on Industrial Electronics, vol. 49, pp. 816-823, April 2002.

[7] Shih-Liang Jung, and Ying-Yu Tzou, "Discrete Sliding-Mode Control of a PWM Inverter for Sinusoidal Output Waveform Synthesis with Optimal Sliding Curve," IEEE TRANSACTIONS Electronics, vol. 11, pp. 567-577, April 1996.

[8] HUO Shao-Cheng, WANG Yong-Ji, "Discrete variable structure controller for a brushless dc motor drive," Proceeding of the CESS, vol. 24, pp. 96-99, June 2004.

[9] SONG Jun-ying, LIU Di-chen, CHEN Yun-ping. "Decentralized variable structure control in asynchronized synchronous generator paralleled with synchronous generator," Proceeding of the CESS, vol. 24,pp.172-178, June 2004.

[10] Jung S, Tzou Y. "Discrete sliding-mode control of a PWM inverter for sinusoidal output waveform synthesis with optimal sliding curve," IEEE Trans. Power Electronics, vol. 11,pp. 567-577, April 1996.

[11] Ramos R, Biel D, Fossas E. A fixed-frequency quasi-sliding control algorithm: application to power inverters design by means of FPGA implementation IEEE Trans. on Power Electronics, vol. 18, pp. 344-355, Jan 2003.

[12] SU Cai-hong, LU yi-min, ZHU Xue- feng. " Variable Structure Control Dc-Dc converter," J. of Wuhan Uni. Of Sci. & Tech. (Natural Science Edition), vol. 26, pp. 169-170, Feb 2003.

[13] WANG Li-qiao, WANG Yong-chang, HUANG Yong-yu, et al. "A Cascade Multi-Level Converter with Phase-Shifted SPWM Technique," High Voltage Engineering, vol. 28,pp. 17~21. July 2002

[14] GAO Wei-bing, The Basic Theory of Variable Structure control, Beijing, China Science Technology Publish, 1990.