Design of SDLC Synchronous Serial Communication Based on Intel 8274

WANG Qi FAN Jianwei CUI Wei YANG Duwei

Department of Aerial Instrument and Electric Engineering

The First Aeronautical Institute of Air Force

Xinyang, China

Fanjianwei_36@sohu.com

***Abstract*—SDLC synchronous serial communication has strong anti-jamming ability and high speed of data transmission, especially suitable for data communication between aircraft piggyback equipment and ground gear under severe condition such as field. To resolve the army demand of maintenance and repair to airborne equipment, the SDLC synchronous serial communication board is developed based on INTEL8274. The feature of the board is high speed data transmission, very strong anti-jamming, well secrecy and so on. The board has good applied effect in aero parameter intelligent testing equipments and aero parameter unloader, and has use value in test control and communication field.**

***Keywords*— ntel 8274, synchronous serial link communication, RS422A**

I. INTRODUCTION

In the course of studying intelligent testing equipment for the system of aero parameter register, to let computer can communicate with the aero parameter equipment, a circuit board was devised. Based on the technology of synchronous serial communication, the board has the function of interrupt and DMA channel trigger.

The INTEL8274 is a kind of multi-procedure communication controller, which has the function of asynchronous (start/stop), byte synchronization and bit synchronization. The INTEL80186 microprocessors are used widely in aircraft flight equipments, INTEL8274 can connect with the CPU of INTEL series, 8237DMA controller and 8259 interrupt controller, which can commute with CPU by inquire, interrupt and DMA model. INTEL8274 is the primary HDLC procedure controller.

II. THE KEY FEATURE AND ULTIMATE COMPOSITION OF INTEL8274

A. The key feature of INTEL8274

- INTEL8274 can be used for asynchronous model, byte synchronization model and bit synchronization model.
- INTEL8274 has two separate full-duplex transceiver.
- INTEL8274 has four separate DMA channel.
- The baud rate can reach to 880kbps.
- INTEL8274 can select bit from 5 to 8; odd check, even check or neither;1,1.5 or 2 stop bit in asynchronous model. The asynchronous model can also detect error for structure, data overlap and check.
- INTEL8274 can select internal or external byte synchronization model, single byte or double byte synchronization, and can check with CRC.

B. The ultimate composition of INTEL8274

A INTEL8274 includes a control logic of system interface, interrupt logic and two full-duplex serial channel. A channel is composed of a group of read-write registers, channel control logic, channel transmitter and channel receiver. The scheme of INTEL8274 is shown in fig 1.

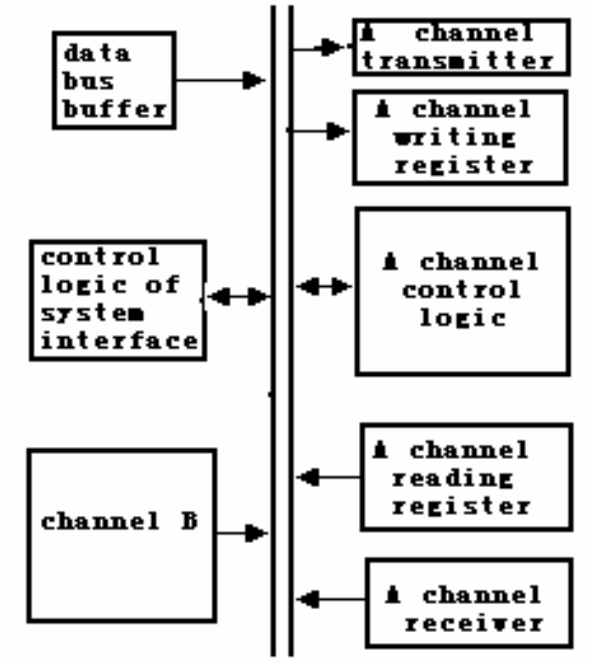

Figure 1. The scheme of INTEL8274

978-1-4244-1674-5/08 /$25.00 ©2008 IEEE CIS 2008

III. INTRODUCE OF SDLC SERIAL COMMUNICATION PROCEDURES

SDLC serial communication procedures are synchronization procedures faced bit, which adopt the combination of some bit to control. The message length is unlimited, the transmission rate exceeds 2400bps. The procedures have very strong capabilities of error correction, anti-jamming and communication security, which are extensively used in the field of military communication control. The communication characters of the procedures are shown in the follow as the table 1:

TABLE I. COMMUNICATION CHARACTER

01111110	A	C	I	FC	01111110

The 01111110 is a symbol character, the procedures prescribe information transmissions must start with the symbol, and end with the same symbol. A information unit which is composed of originating marker and end mark is called a frame. All information are transmitted with frames in SDLC.

After the start symbol character, there are a 8 bit address field, a 8 bit control field, a information field and a 16 bit frame check field. The bit length of information field is alterable.

If the transmitted information is the same as the start symbol character, the SDLC uses the technology of bit 0 insert/delete, which resolved the problem of transparence in transmit process. If there are some questions in send process, the SDLC will transmit seven bit 1 continuously as a disabled character to let the frame invalidation.

The check of SDLC frame uses CRC, the code is a 16 bit frame check sequence following the information field. The CRC polynomial is 16+X*124*5+X*1.

IV. THE HARDWARE DESIGN OF SDLC BOARD

When the aero piggyback data equipments were checked and maintained with universal computer, the transmitted information of SDLC serial communication is very much, using the I/O bus of computer to memory and deal with transmitted data cannot achieve well effect. The SDLC board use the 8274 as the main control chip, make use of DMA of computer and software inquiry mode, accomplishes data transmit and disposal rapidly with half duplex mode.

V. THE COMPOSITION OF SDLC BOARD HARDWIRED CONNECTION

The composition of hardwired connection is shown in figure 2.

The interface connecting to external device also can let the clock synchronization, except receive and transmit data. Port unit is composed of AM26LS31 and AM26LS32, adopts differential connection mode which meet the demand of RS-422A.

The frequency I/O bus is 8MHz, the operating frequency of INTEL8274 is 4MHz. Using frequency division from I/O bus can obtain the operating frequency of INTEL8274. The output frequency of the board is adjustable 125 KHz. The chip selection signal of 8274 is given by I/O bus, The A1 and A2 of I/O bus can select internal register of 8247 and set the I/O address of the board. The address is adjustable from 0X380 to 0X386.

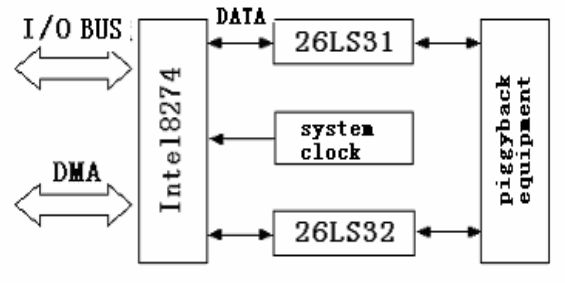

Figure 2. The block diagram of SDLC serial board

The working of the board is inquiry mode, always is in the channel receive. When there is some information to be received of transmitted, the software changes working, lets the DMA channel of computer as receive and transmit channel through DMA request trigger. The board includes the follow four circuits:

- Clock generates and control circuit. The circuit is composed of quartz crystal (8MHz), clock generator MD8284 and frequency divider, which provides the circuit work with system clock and data transmitting with shift impulse.
- Multiprotocol controller INTEL8274. It accomplished the conversion about serial data and parallel data, generates and identifies symbol field, searches and identifies address field, generates CRC check code and check CRC, provides interrupt vector, touches off DMA and so on.
- Coding circuit, which is composed of dial code switch, address comparator 74LS688 and so on, provide the circuit necessary address.
- Data level conversion circuit, which is composed of RS-422A, AM26LS31 driver and AM26LS32 receiver, accomplishes interconversion between TTL level and RS-422A level.

VI. THE SOFTWARE DESIGN OF SDLC BOARD

The software of the board is a memory-resident program based on DOS operating environment, which can make the best of the hardware resource. The software adopts C++ programming language. Its flow chart is shown in figure 3, which is mostly composed of system initialization, send data, receive data, data check and data disposal.

A. System initialization

The initialization program includes the initialization of INTEL8274, DMA controller and setting buffer.

- Initialization 8247 core control chip. This includes resetting channel A and channel B, selecting of SDLC

serial synchronous communication mode, writing SDLC symbol character to register, creating the address of receive system; define separately the working of channel A and channel B. The channel A uses DMA transmission mode.

- Initialization DMA working includes clearing the DMA trigger and writing period.
- Setting buffer, this includes setting a output buffer 32 bytes in length and writing first address of the buffer into page register and address register of DMA3, writing 32 into byte counter, setting a input buffer 1K bytes in length and writing first address of the buffer into page register and address register of DMA3, writing 1K into byte counter.

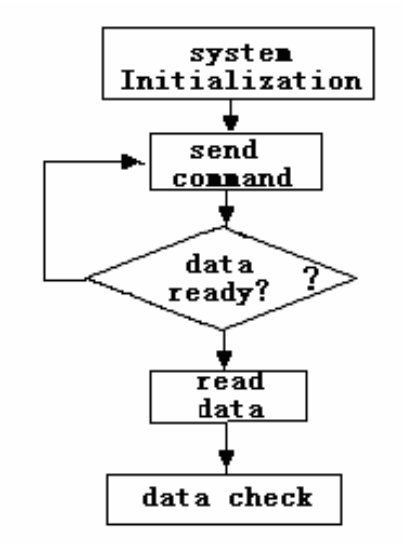

Figure 3. Software flow chart of SDLC

B. Sending data

Sending data includes opening DMA3 mask, resetting INTEL8274 external register and error register, sending address field, sending transmitted data number of bits, sending SDLC frame check polynomial, sending data RTS, masking CPU, reading RR1 register of INTEL8274, diagnosis transmitted information, giving suggestion information and dispose method.

C. Receiving data

Receiving data includes reading NTEL8274 RR0 register, judging if the received byte is available, opening DMA mask receiving data, reading INTEL8274 RR1 register, diagnosis transmitted information, giving suggestion information and dispose method.

D. Data processing.

When data receiving is over, data processing program will process the data in butter, and displaying the result.

VII. CONCLUSION

The thesis introduced serial communication regulation of multi-regulation serial communication controller Intel 8274 and SDLC, and expatiated the hardware and software design of serial synchronous communication board based Intel 8274.

REFERENCE

[1] MAKINO E, MITSUYA T, SHIBATA T. Dynamic actuation properties of TINI shape memory diaphragm. Sensors and Actuators, 2000(79): 128-135.

[2] NI. IEEE-488 Interface Boards User's Manual [Z].

[3] Puschell J J, Bayse R, High data rate ultraviolet communication systems for the tactical battlefield [Z]. TITAN Systems 5910 Pacific Center Bouleward San Diego, California, 1990.