Input Delay Compensation with Digital Redesigned A/D Conversion

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Abstract — **Network controlled system will always experience some delays in communications, and how to improve its stability is of great importance for industry applications. In this paper, one novel method of delay compensation by utilizing digital redesign is proposed. First, analog controller is designed for the delay free system, and then the delay compensation algorithm is modulated through A/D conversion. In addition, this method can deal with delay variations by adjusting PAM controller period. The proposed methodologies have been testified through MATLAB/Simulink, and the simulation results effectively confirmed its theoretical correctness.**

Keywords — ***Digital Redesign, Input Delay, Pulse Amplitude Modulation, Network Control***

I. INTRODUCTION

Network controlled system can effectively reduce wiring, and achieve low installation cost, ease of maintenance, and flexibility in reconfiguration [1]. This kind of implementation can be conveniently used in the complex industrial systems such as machine center, power plant, as well as petrochemical processing facilities, where an array of sensors, actuators and controllers need to interactively exchange data [2]. Meanwhile, network control imposes a serious challenge for the controller design, since the inevitable and unpredictable communication delay and data loss may degrade the performance, or even destabilize the system [3]. Therefore, how to develop an applicable delay compensation algorithm is of great importance for the industry applications.

Today almost all the control systems are realized with digital devices; whereas most dynamical systems are formulated in a continuous-time framework. The resulting digitally controlled analog system constructs a mixed-signal system, or hybrid system. Digital controller design for mixed-signal system becomes an active research topic for system and control area, since the simple mixture of different types of signals may seriously deteriorate performance [4]. On the other hand, the hybrid system also provides a platform for the designer to utilize respective advantages of different signals in achieving performance improvement like delay compensation.

In the design, one common approach is direct digital design: first discretize the analog plant through z-transform, and then make the discrete-time design for the discretized plant, or the digital controller is obtained in discrete time domain directly. Another approach is called as digital redesign [5]: first an analog controller is designed, and then redesigned to the digital one. Digital redesign is to convert the analog control signal to digital control signal through some certain method. For example, bilinear transform is the most famous digital redesign method. In such a way, digital controller is obtained through a two-step procedure: first to find the analog controller in continuous domain, and then translate it into its digital counterpart in discrete domain. In physical implementation, generally the digital controller realization can be categorized into two modes. One is PAM (Pulse Amplitude Modulated) controller, which produces a series of piecewise-constant continuous pulses with variable amplitude but fixed pulse width. The other is PWM (Pulse Width Modulated), which provides a series of discontinuous pulses with fixed amplitude but variable pulse width [6].

Most conventional digital controller design methods, no matter direct digital design or digital redesign, are commonly employed to design PAM controller but not PWM controller. However, in recent years, due to the impressive performances in efficiency and noise immunity, together with the popularity of power converter and real-time embedded controller like DSP (Digital Signal Processor), PWM devices have gradually become the mainstream products in on-off control, power converters, motor drive, etc [7]. The mismatch between design methodology and physical implementation causes an interesting phenomenon that PAM controller is probably realized through PWM device.

The principle of equivalent area is commonly employed to make the controller signal translation from analog to digital [6]. Obviously, the smaller the switching period, the smaller conversion error is. It is also corresponding with the current technology trend that the sampling and switching frequency in digital system is more and more faster. However, short controller period is not always beneficial, because there do exist some instances where a longer controller period is better. For example, even a small input delay is rather significant compared with the fast PWM switching rate, leading to complicated and time-consuming calculations. However, the same time delay, if describe with the longer period in PAM, it may be only a fraction of the controller period, such that the predication compensation can be significantly simplified.

In conclusion, if designer can appropriately design the digital controller in PAM with a long period, and then

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modulate the control signal to PWM device with a short period, then resulting system can take advantages of both sides in some certain circumstances like time delay.

II. PREDICTION-BASED DIGITAL REDESIGN

Digital redesign was originally developed when digital controllers are emerging to replace existing analog controllers [8]. This technique can effectively minimize the conversion error to satisfy the requirements of then slow controller and sampling rate. Among those digital redesign methodologies in literature, one commonly employed principle in controller conversion is "equivalent area" [9].

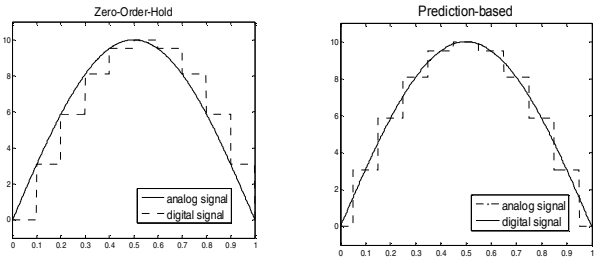

Figure 1. A/D conversion with ZOH and Prediction-based Digital Redesign

In this paper, the prediction-based digital redesign [10] technique is utilized. This technique has been testified to be insensitive to numerical errors, also can be conveniently adjusted to make the state matching at different time instant which is crucially important for time delay compensation. To illustrate the idea of prediction-based digital redesign, two kinds of A/D signal conversion techniques are compared in the above Figure 1. The left one shows the result with Zero-Order-Hold, obviously the area covered by analog signal and digital signal are different. Especially when sampling period is long, the conversion error will be too significant to be ignored. If the digital signal achieved after Zero-Order-Hold can be shifted to the left by a half period as the right one in Fig. 1, then the conversion error will be effectively reduced. Following this idea, the predication-based digital redesign can be described as:

Consider a linear controllable continuous-time system

$$\dot{x}_c(t) = Ax_c(t) + Bu_c(t), \quad (1)$$

where A and B are constant matrices of appropriate dimensions. Let the continuous-time state-feedback controller be

$$u_c(t) = -K_c x_c(t) + E_c r(t) \quad (2)$$

Then the controlled system is

$$\dot{x}_c(t) = (A - BK_c)x_c(t) + BE_c r(t) \quad (3)$$

Let the state equation of a corresponding hybrid model be

$$\dot{x}_d(t) = Ax_d(t) + Bu_d(t), \quad (4)$$

where $u_d(t)$ is a piecewise-constant input vector, satisfying

$$u_d(t) = u_d(kT) \quad \text{for } kT \le t < (k+1)T$$

and T is the sampling period. Let the discrete-time state-feedback controller be

$$u_d(kT) = -K_d x_d(kT) + E_d r^*(kT) \quad (5)$$

where K_d is a digital state-feedback gain, E_d is a digital feedforward gain, and $r^*(kT)$ is a piecewise-constant reference input vector to be determined in terms of $r(t)$ for tracking purpose. The digitally controlled closed-loop system thus becomes

$$\dot{x}_d(t) = Ax_d(t) + B[-K_d x_d(kT) + E_d r^*(kT)] \quad (6)$$

for $kT \le t < (k+1)T$.

The state $x_c(t)$ in (1) at $t_v = KT + vT$ for $0 \le v < 1$, is found to be

$$x_c(t_v) = \exp(A(t_v - kT))x_c(kT) + \int_{kT}^{t_v} \exp(A(t_v - \tau))Bu_c(\tau)d\tau$$
$$= G^{(v)}x_c(kT) + H^{(v)}u_c(t_v), \quad (7)$$

where $u_c(t_v)$ is a piecewise-constant input, and

$$G^{(v)} = \exp(A(t_v - KT)) = (\exp(AT))^v,$$
$$H^{(v)} = \int_0^{vT} \exp(A\tau)Bd\tau = \left[G^{(v)} - I_n\right]A^{-1}B.$$

In order to minimize the conversion error, it is necessary to have $u_d(kT) = u_c(t_v)$. This leads to the following prediction-based digital controller:

$$u_d(kT) = u_c(t_v) = -K_c x_c(t_v) + E_c r(t_v). \quad (8)$$

Substituting the predicted state $x_d(t_v)$ in (7) into (8) and then get

$$u_d(kT) = (I_m + K_c H^{(v)})^{-1}[-K_c G^{(v)} x_d(kT) + E_c r(t_v)]. \quad (9)$$

For simplicity, it can be expressed as

$$u_d(kT) = -K_d^{(v)} x_d(kT) + E_d^{(v)} r^*(kT), \quad (10)$$

where $K_d^{(v)} = (I_m + K_c H^{(v)})^{-1} K_c G^{(v)}$, $E_d^{(v)} = (I_m + K_c H^{(v)})^{-1} E_c$.

Actually the tuning parameter v can be adjusted between 0 and 1 to minimize the conversion error [10]. To simplify the algorithm, v is fixed to be 0.5 in this paper, which means the digital control signal is shifted to left by a fixed half period as shown in Fig. 1.

III. DELAY-FREE SYSTEM CONTROLLER DESIGN

Digital redesign follows a two-step procedure. This section III is the about analog controller design for the delay free system, and then the next section IV is about the delay compensation.

Let the state space model of the plant model $G_1(s)$ be

$$\dot{x}_1(t) = A_1 x_1(t) + B_1 u_1(t), \quad (11a)$$
$$y_1(t) = C_1 x_1(t), \quad (11b)$$

where A_1, B_1, C_1 are constant matrices of appropriate dimensions. The state space model of the cascaded controller $G_2(s)$ can be written as

$$\dot{x}_2(t) = A_2 x_2(t) + B_2 u_2(t), \quad (12a)$$
$$y_2(t) = C_2 x_2(t) = u_1(t), \quad (12b)$$
$$u_2(t) = -y(t) + E_c r(t), \quad (12c)$$

where A_2, B_2, C_2, E_c are constant matrices of appropriate dimensions.

The digital redesign is realized through state space model, therefore the above cascaded system needs to be integrated into one model. To achieve this aim, formulate the closed-loop

cascaded systems (11) and (12) with $d(t)=0$ into an augmented system as

$$\dot{x}_e(t) = A_e x_e(t) + B_e u_1(t) + E_e\, r(t), \qquad (13a)$$

$$y_e(t) = y_1(t) = C_e x_e(t), \qquad (13b)$$

where

$$A_e = \begin{bmatrix} A_1 & 0 \\ -B_2C_1 & A_2 \end{bmatrix},\ B_e = \begin{bmatrix} B_1 \\ 0 \end{bmatrix},\ E_e = \begin{bmatrix} 0 \\ B_2E_c \end{bmatrix},$$

$$x_e = \begin{bmatrix} x_1(t) \\ x_2(t) \end{bmatrix},\ C_e = [C_1\ \ 0]\ ,$$

and (A_1, B_1, C_1), (A_2, B_2, C_2) are state space model of plant and controller, respectively. Note if there exist *D* term in the state space model of either plant or controller, it can also be included as shown in [11]. The resulting state-feedback LQR for the augmented system (13) can be chosen as

$$u_1(t) = -K_e x_e(t) = -K_1 x_1(t) - K_2 x_2(t), \qquad (14)$$

where K_1 and K_2 are of appropriate size to match A_1 and A_2 respectively.

This method has been successfully utilized to Multi-Input-Multi-Output (MIMO) system design, and there are detailed descriptions about how to determine the PID controller parameters in [12]. For example, if the plant model is a Single-Input-Single-Output (SISO) second-order system, actually the plant states feedback (i.e. $K_1 x_1(t)$ in (14)) act as proportional controller and derivative controller respectively. If initially set $G_2(s)$ to be integer only, then K_2 can be regarded as the gain of the integer controller. Thus, the total control law in (14) is equivalent to a PID controller [13]. Once the optimal control law is obtained, then the designed closed-loop system becomes

$$\begin{bmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \end{bmatrix} = \begin{bmatrix} A_1 - B_1K_1 & -B_1K_2 \\ -B_2C_1 & A_2 \end{bmatrix} \begin{bmatrix} x_1(t) \\ x_2(t) \end{bmatrix} + \begin{bmatrix} 0 \\ B_2E_c \end{bmatrix} r(t) \qquad (15a)$$

$$y_1(t) = C_1 x_1(t). \qquad (15b)$$

The block diagram of the designed augmented system (13) including the controller (14) is shown in Fig. 2.

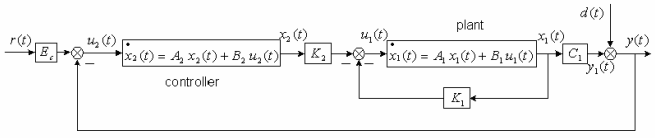

Figure 2. Analog Controlled System

IV. TIME DELAY COMPENSATION

As shown in the Fig. 3 [14] below, both input delay and output delay are existing in the network controlled system, also known as actuator delay or sensor delay. Through appropriate mathematical transformation, input delay and output delay can be allocated to either input or output or their combinations at the designer convenience [15], and its controller implementation for the modified model can be realized through a virtual observer [16].

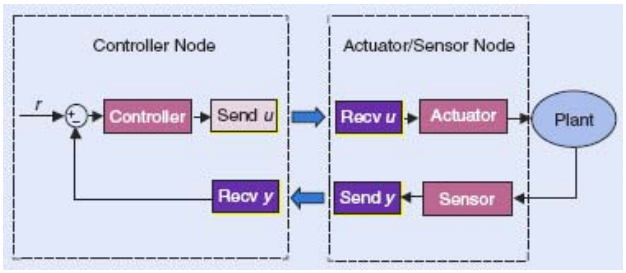

Figure 3. Time Delays in Network Control [14]

To simplify the description in this paper, we assume some certain network controlled system has been simplified with the input delay only, as shown in the following Fig. 4. To clarify the continuous-time signal and discrete-time signal, we use subscript *d* to indicate the digital signals in the following derivations.

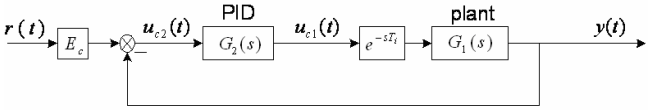

Figure 4. Input Delayed System with Cascaded Controller

Suppose the controller period is *T*, and the input delay is T_i. Let $t_v = kT + vT$, and $T_i = rT$ with a delay fraction number r. And as mentioned before, *v* is fixed to be 0.5 in this paper. To compensate the input delay, the predicted analog controller at $t = t_v$ for the augmented input-delay system in (14) is given as

$$u_1(t_v) = -K_1 x_1(t_v + T_i) - K_2 x_2(t_v + T_i), \qquad (16)$$

where predicted inter-sampling state $x_{d1}(t_v + T_i)$ of the plant with input-delay [4] can be obtained as

$$x_{d1}(t_v + T_i) = x_{d1}[kT + (r+v)T]$$

$$= G_1^{(v+r)} x_{d1}(kT) + H_1^{(v+r)} u_{d1}(kT - T) + H_0^{(v+r)} u_{d1}(kT), \qquad (17)$$

where $G_1^{(v+r)} = e^{A_1(v+r)T}$, $H_1^{(v+r)} = G_1^{(v)}[G_1^{(r)} - I_{n1}]A_1^{-1}B_1$, and $H_0^{(v+r)} = [G_1^{(v)} - I_{n1}]A_1^{-1}B_1$.

The predicted inter-sampling state $x_{d2}(t_v + rT)$ of the delay-free controller is

$$x_{d2}(t_v + rT) = x_{d2}[kT + (v+r)T]$$

$$= G_2^{(v+r)} x_{d2}(kT) + H_2^{(v+r)} u_{d2}(kT). \qquad (18)$$

Substituting (17), (18) into (16), and yields

$$u_{d1}(kT) = -K_{d11} x_{d1}(kT) - K_{d12} x_{d2}(kT) - D_{d11} u_{d1}(kT - T) - D_{d12} u_{d2}(kT) \qquad (19)$$

where

$$K_{d11} = (I + K_1 H_0^{(v+r)})^{-1} K_1 G_1^{(v+r)},\ K_{d12} = (I + K_1 H_0^{(v+r)})^{-1} K_2 G_2^{(v+r)},$$

$$D_{d11} = (I + K_1 H_0^{(v+r)})^{-1} K_1 H_1^{(v+r)},\ D_{d12} = (I + K_1 H_0^{(v+r)})^{-1} K_2 H_2^{(v+r)}.$$

On the other hand, the delay-free controller, at the inter-sampling instant $t = t_v$, it is necessary to have

$$u_{d2}(kT) = u_2(t_v) = -C_1 x_1(t_v) + E_c r(t_v)$$

$$= -C_1 x_{d1}(t_v) + E_c r(kT), \qquad (20)$$

where the solution $x_{d1}(t_v)$ of the plant with input-delay is

$$x_{d1}(t_v) = x_{d1}(kT + vT)$$

$$= G_1^{(v)} x_{d1}(kT) + H_1^{(v)} u_{d1}(kT-T) + H_0^{(v)} u_{d1}(kT) \quad (21)$$

where $G_1^{(v)} = e^{A_1 vT}$, $H_1^{(v)} = G_1^{(v-r)}[G_1^{(r)} - I_{n1}]A_1^{-1}B_1$, $H_0^{(v)} = [G_1^{(v-r)} - I_{n1}]A_1^{-1}B_1$. Note if $v < r$, then the input vectors are $H_1^{(v)} = [G_1^{(v)} - I_{n1}]A_1^{-1}B_1$, $H_0^{(v)} = 0$.

The digital controller $u_{d2}(kT)$ can be generated by substituting (21) into (20) to get

$$u_{d2}(kT) = u_2(t_v) = -y_{d1}(t_v) + E_c r(kT)$$
$$= -K_{d21}x_{d1}(kT) - K_{d22}x_{d2}(kT) - D_{d21}u_{d1}(kT-T) + E_{d2}r(kT) \quad (22)$$

where

$$K_{d21} = (I - C_1H_0^{(v)}D_{d12})^{-1}(C_1G_1^{(v)} - C_1H_0^{(v)}K_{d11}),$$
$$K_{d22} = (I - C_1H_0^{(v)}D_{d12})^{-1}(-C_1H_0^{(v)}K_{d12}),$$
$$D_{d21} = (I - C_1H_0^{(v)}D_{d12})^{-1}(-C_1H_0^{(v)}D_{d11} + C_1H_1^{(v)}),$$
$$E_{d2} = (I - C_1H_0^{(v)}D_{d12})^{-1}(-C_1H_0^{(v)}E_{d1} + E_c).$$

Thus, the digitally redesigned sampled-data input-delay system becomes

$$\dot{x}_{d1}(t) = A_1x_{d1}(t) + B_1u_{d1}(t-T_i),$$
$$u_{d1}(kT) = -K_{d11}x_{d1}(kT) - K_{d12}x_{d2}(kT) - D_{d11}u_{d1}(kT-T) - D_{d12}u_{d2}(kT),$$
$$y_{d1}(t) = C_1x_{d1}(t),$$

and

$$x_{d2}(kT+T) = G_2x_{d2}(kT) + H_2u_{d2}(kT),$$
$$u_{d2}(kT) = -K_{d21}x_{d1}(kT) - K_{d22}x_{d2}(kT) - D_{d21}u_{d1}(kT-T) + E_{d2}r(kT),$$
$$y_{d2}(kT) = K_{c2}x_{d2}(kT) + D_{d12}u_{d2}(kT).$$

The structure of the digitally redesigned sample-data input-delay system is shown in Fig. 5.

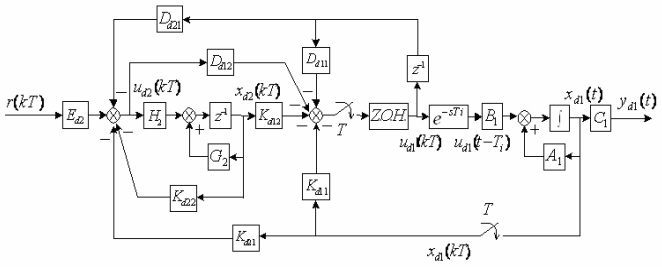

Figure 5. Digital Redesigned A/D Implementation

V. SIMULATION RESULTS

Suppose a supply air pressure loop with varied delay [17] is described as:

$$G(s) = \frac{0.81}{(0.97s+1)(0.1s+1)}e^{-T_i s} \quad (23)$$

For such a second-order SISO system, its PID controller design can be made through LQR, and get $K_1 = [1.0836 \quad 7.5403]$ and $K_2 = [-1]$, where the plant states feedback gain vector K_1 acts as proportional controller and derivative controller respectively, and K_2 can be regarded as the gain of the integer controller.

In this paper, the simplified methodology can only deal with the delay less than one PAM controller period. If the delay is increased, its compensation can be realized by prolonging the PAM period. Since the controller parameters in Fig. 5 are static, the PAM period variation will not considerably increase the real-time calculation burden. For example, if the delay $T_i = 0.5s$, let PAM period to be $T = 1s$, such that the result is:

$$K_{d11} = [0.1941 \quad 1.9406],\ K_{d12} = [-0.7597],$$
$$K_{d21} = [0.5498 \quad 5.5539],\ K_{d22} = [0].$$
$$D_{d11} = [0.1271],\ D_{d12} = [-0.7597],\ D_{d21} = [0.2713].$$

If the delay is further increased to $T_i = 1s$, then prolong the PAM period to be $T = 1.5s$, such that the result is:

$$K_{d11} = [0.0836 \quad 0.8356],\ K_{d12} = [-0.7088],$$
$$K_{d21} = [0.4292 \quad 4.2956],\ K_{d22} = [0].$$
$$D_{d11} = [0.1462],\ D_{d12} = [-1.2405],\ D_{d21} = [0.3932].$$

The following Fig. 6 demonstrates the output response, in which solid line refers to the delay free system, dotted line refers to the A/D conversion with Zero-Order-Hold only, and dash-dot line refers to the A/D conversion with digital redesign. Obviously, the compensation mechanism works effectively.

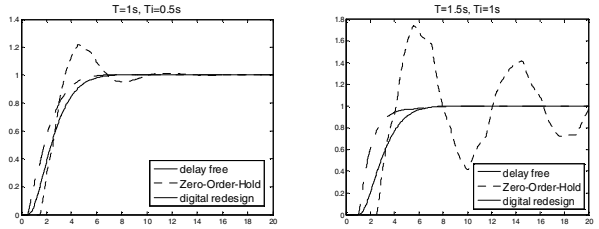

Figure 6. Output Performance with Different A/D conversions

If $T_i = 1.5s$, and then select $T = 2s$, at this moment A/D conversion with Zero-Order-Hold can not stabilize the system anymore. Whereas, digital redesign can still give a satisfied performance and its parameters are:

$$K_{d11} = [0.0367 \quad 0.3667],\ K_{d12} = [-0.674],$$
$$K_{d21} = [0.332 \quad 3.3207],\ K_{d22} = [0].$$
$$D_{d11} = [0.1314],\ D_{d12} = [-1.685],\ D_{d21} = [0.4879].$$

Finally, if the delay $T_i = 2s$, then choose the PAM period to be $T = 2.1s$, such that the result is:

$$K_{d11} = [0.0206 \quad 0.2063],\ K_{d12} = [-0.6684],$$
$$K_{d21} = [0.3154 \quad 3.1539],\ K_{d22} = [0].$$
$$D_{d11} = [0.1373],\ D_{d12} = [-2.0387],\ D_{d21} = [0.5041].$$

In circumstances with long delay, analog controlled system can perform better than simple A/D conversion with Zero-Order-Hold, but appropriately redesigned digital controller can achieve a much better performance than analog controller. As shown in Fig. 7, solid line refers to the delay free system, dotted line refers to the analog controlled delayed system, and dash-dot line refers to that of digital redesign.

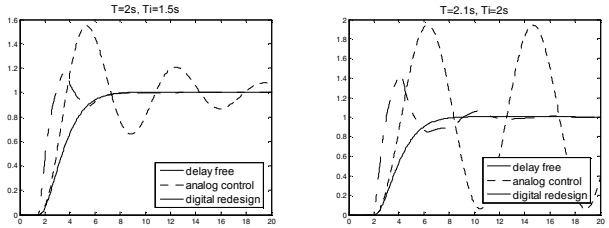

Figure 7. Output Performance with Long Delay

VI. CONCLUSIONS

This paper addressed a novel delay compensation methodology with digital redesigned A/D conversion. The advantages include: Controller design is separated from the delay compensation; Controller period can be adjusted to cope with delay variation; Meanwhile its computational burden is moderate for real-time applications. The simulation result testified the theory correctness very well, and physical implementation on MIMO (Multi-Input-Multi-Output) system is on the way.

ACKNOWLEDGMENT

This work was supported in part by US Army Research Office Grant #W911NF-06-1-0507 and NSF Grant #0717854.

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