Design of a DSP-based CMOS Imaging System for Embedded Computer Vision

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***Abstract*—With the advance of image processing techniques and the fast reduction of image sensor costs, embedded computer vision is becoming a reality. This paper presents the design and implementation of an integrated CMOS imaging system based on DM642. The system can acquire VGA resolution image at 100frame/s. The on-board 10Mbps Ethernet connection and the UART as well as digital I/O ports provide convenience for direct interface to other intelligent devices. The on-board software provides image acquisition function, network-based control, network-based data transfer, JPEG compression, image pre-processing functions, edge detection function. Automatic exposure control and automatic white balance are realized in the system. Experiments show that the CMOS imaging system has a good performance in terms of imaging quality, with much potential for being used as intelligent vision system.**

Keywords—CMOS Imaging System, DM642, Embedded Computer Vision

I. INTRODUCTION

Image acquisition system is the front end of all machine vision system. There are two groups of sensing devices used in electronic imaging system: charge-coupled device (CCD) sensor and complementary metal oxide semiconductor (CMOS) sensor. During the past decade, the CMOS sensors have experienced a great improvement in both imaging quality and frame transfer rate ([1]-[4]).

With the relative lower cost of imaging sensors and the ease of integrating CMOS-based sensor modules into the CMOS-based processor units, embedded vision applications are becoming a more and more important area. In comparison to CCD sensors, the CMOS sensor has the advantages of lower power, smaller size, faster data output rate and ease of control. These advantages make CMOS sensor more suitable for embedded applications. Both industry and research institutes have shown great interests on embedded vision applications. The recently-emerging smart cameras (or intelligent vision sensors) are a kind of embedded vision systems. Companies playing a role in the market of smart camera, to name a few, include Vision Components from Germany, DVT Sensors and Cognex Inc. from US, Matrox Imaging from Canada, and many others [5].

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The hardware architectures for the embedded vision applications are diverse, ranging from DSP to FPGA, and to the combination of both [6]. A reconfigurable hardware structure of 'smart camera' by incorporating a high quality video camera with a FPGA processing board is shown in [7]. The system shows a more than 20times speedups in medical image processing application and fluid dynamics application, in comparison to the PC-based vision system. Sun presents the design of embedded real-time image acquisition system based on CPLD and a TMS320C6205, where the CPLD is used for image acquisition and delivery logic control, and the DSP is used for image processing function [8]. The video signal comes from a CCD camera and captured by a video processing chip SAA7113. The resolution of outputting image is 512x512 pixels. The output frame rate of the system is not stated clear in the paper. An image processing system based on TMS320VC5416 and OV7640 (a 640x480 CMOS sensor) is presented in [9]. The image data from CMOS sensor is ported to an FIFO chip and then passed to the DSP for image processing. An on-board CPLD is used for the image data read/write control. The output frame rate is 5 frames per second. The system is used for the estimation of boarding passengers of a public transportation bus during the daily operations.

II. HARDWARE DESIGN

As the CMOS sensor technology evolves fast, mother-daughter structure is adopted for PCB board design. The mother board hosts the DSP processor and relevant peripherals, including a CPLD, a 4MByte Flash, 2x 32MByte SDRAM, USB2.0 interface and Ethernet interface IC. The daughter board hosts the image sensor and an on-board C Mount adapter for optical lens. The daughter board is attached to the mother board via a PCB-mounted 180pins connector. A block diagram of the hardware design is shown in Figure 1.

A. DM642

TMS320DM642 is the second generation digital signal processor from TI dedicated to media processing. The internal core of DM642 is C64x CPU. As a media processor, DM642 configures 3 video ports (VP0, VP1, VP2), providing convenience for the integration of multiple media sources. Each video port is capable of sending and receiving digital video data, capturing and displaying raw data. The Ethernet media access controller (EMAC) provides a fast and convenient data interface between processor and network.

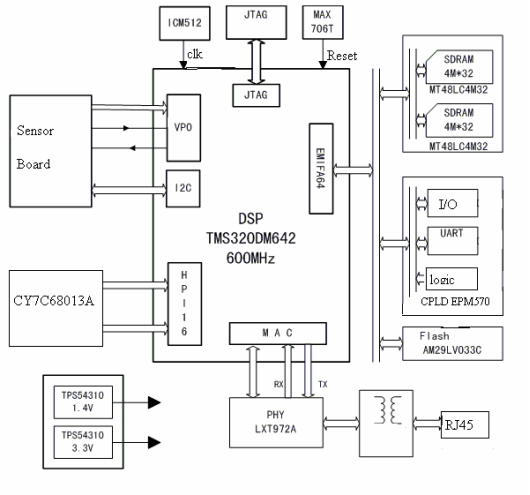


Figure 1. Diagram of the CMOS Imaging System

B. CMOS Sensor

The CMOS image sensor used in this system comes from Micron Technology. The sensor is programmable through a simple two wire serial interface. The image sensor is amounted on a separate board for the convenience of exchange.

C. Principle

The working principle of the CMOS imaging system is as follows. The raw RGB data from the CMOS image sensor is directly ported to the VP0 of DM642, and are then transferred to SDRAM via internal peripherals using EDMA service. Due to the huge size of image data, two 133MHz 4Mx32Bit SDRAM, totally 64MB memory are adopted in the system. The 133MHz clock comes from a frequency multiplier ICS512M, which is driven by an on-board 25MHz oscillator. Another on-board oscillator provides a 50MHz clock signal to the CLKIN pin of DM642. The clock signal is multiplied using the in-chip PLL controller to generate the 600MHz CPU clock.

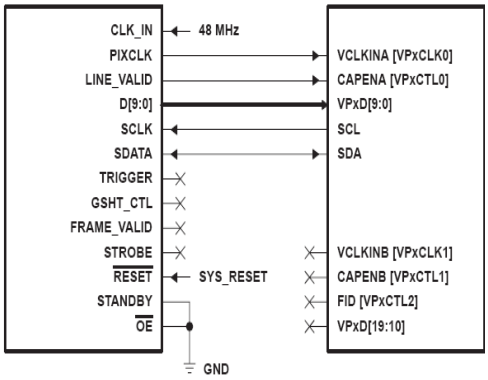


Figure 2. The interface of CMOS sensor to DSP

The Boot up mode of TMS320DM642 is EMIFA. A 4MB flash is placed on the board for program storage. When DM642 is powered on, the system will automatically load the code put on the beginning session of the flash. To satisfy the high-speed data output need of most vision applications, the system has incorporated both USB2.0 and Ethernet data interface. A CY7C68013A from Cypress is used for the USB interface. CY7C68013A is interfaced to DM642 via HPI. As a host device, the USB chip can access all the data in the data space of DM642. On the other hand, DM642 has integrates an EMAC controller. Hence, the Ethernet communication link can be realized by directly including a physical-level IC. LXT972A is used in the system. To provide convenience for direct interfacing embedded vision system to the actuators, sensors and controllers, eight digital I/Os and one serial port are realized in the system. Both digital I/Os and the UART function are implemented using the on-board EPM570.

The power supply of the system is 12V DC. Two kinds of voltages are needed in the system: 3.3v for the peripherals and 1.4v for DSP. Two DC/DC voltage converters with SWIFTTM (TPS54310) are included in the system to achieve 1.4V and 3.3V voltage separately.

III. SOFTWARE DESIGN

In comparison to the hardware design task for a DSP-based vision system, the task of software design is more demanding. To make the CMOS imaging system an appropriate platform for embedded vision application, both system and application level of software are provided.

A. System software

The system level software design is based on the DSP/BIOS provided by TI. DSP/BIOS is a scalable real-time kernel, providing functions such as preemptive multi-threading, hardware abstraction, real-time analysis and configuration tools. The components of the system level software are shown in Figure 3, where DSP/BIOS is the core of whole system software.

The low-level drivers, which have a standard interface to up-level system, are responsible for the driving and management of specific hardware on board. For examples, VP mini-driver realizes the driving and management function of DM642 video port; CMOS sensor mini-driver realizes the driving and management function of CMOS sensor. The task modules that are supported by the real-time kernel complete different application tasks.

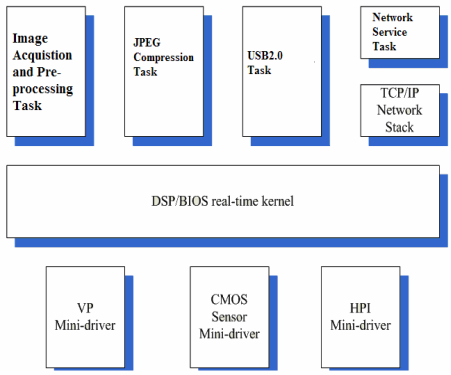


Figure 3. Components of System Level Software

In DSP/BIOS, a device driver is implemented in two levels. At the upper level is the class driver, which is independent of device and provides the functions of multi-

threading serialization, synchronization of services, and management of device instances. There are three kinds of class drivers in DSP/BIOS: SIO, PIP and GIO. In this system, the GIO class driver is implemented. At the lower level is mini driver. The class driver call specific mini driver, which is related to hardware, to complete the hardware functions. The mini driver has a standard IOM mini-driver interface. With the IOM interface, the GIO class driver can access the specific hardware easily using a parameter table.

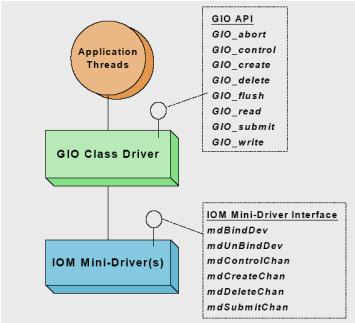


Figure 4. Relation between GIO and mini-driver

B. Application software

For this CMOS imaging system, the targeted application areas are vision-based surveillance and mobile robots. The application software is categorized into four groups: general tasks, image pre-processing tasks, feature extraction tasks, and high-level image understanding tasks. General application tasks include network control, image acquisition, and image compression. The image pre-processing tasks refer to procedures of noise reduction, format conversion, color correction, automatic white-balance, gamma correction, dark illumination correction, and image contrast enhancement, etc. Feature extraction tasks refer to the implementation of classical edge detectors, morphology operators and blob analysis. These three parts are essential for most vision-based applications. The high-level object recognition and image understanding tasks are more application related, hence beyond the scope of this project.

Network-based camera control and data transfer functions are implemented using APIs in Network Developers' Kit. The image acquisition function is realized using the video port VP0, which is configured to work on video capture mode. We use APIs in DSP/BIOS (FVID_create(), FVID_control(), FVID_alloc(), FVID_exchange(), etc.) to acquire the video data from CMOS sensor. The acquisition rate is about 100 frames (VGA format) per second. The on-board JPEG encoder can compress selected frames and pass the compressed images to a computer via network.

For image pre-processing functions, we have realized automatic exposure control, automatic white-balance, gamma correction, and Gaussian smooth filter on the platform. Automatic exposure control is realized based on the analysis of green component values of raw data. If the number of saturated pixels is greater than 70%, it is considered over exposure. The integration time is reduced by half. On the other hand, when the number of dark pixels is greater than 10%, it is considered under exposure, and the pixel integration time is increased by two times. Automatic white balance (AWB) is realized through detecting gray points in the image. The average gray value of these points in the image (avg_Gray) is calculated. Then the average values of R, G, B components of these points in the image are computed. The correction coefficients are obtained using the following formula:

$$r\_coef = \frac{avg\_Gray}{avg\_R} \quad (1)$$

$$g\_coef = \frac{avg\_Gray}{avg\_G} \quad (2)$$

$$b\_coef = \frac{avg\_Gray}{avg\_B} \quad (3)$$

These coefficients multiply the red, green and blue pixel values respectively to obtain the balanced image.

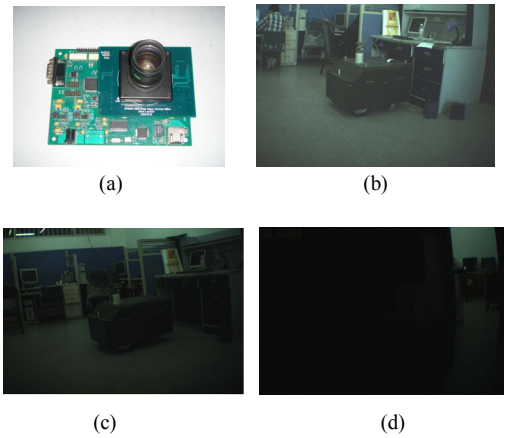
(a) (b)

Figure 5 Original Image (a) and Image after AWB (b)

For feature extraction tasks, we have implemented the edge detection algorithm.

IV. Experiments and Results

The CMOS imaging system with lens attached and the acquired images are shown in Figure 6. The system has been tested under various illuminating conditions. With the natural sunlight illumination in day time, the image acquired indoor shows a good clarity. However, the images acquired at night are not very satisfying .



(a) (b)

(c) (d)

Figure 6 CMOS Imaging System and Sample Images. (a) CMOS imaging system; (b) Image acquired at day time; (c) Image acquired at night with ceiling lighting; (d) Image acquired at night without ceiling lighting.

The raw data from image sensor is sent to the video port directly. As each video port is capable of capturing/displaying

data independently, the CPU of DM642 can concentrate on image preprocessing functions. The execution time of edge detector and JPEG encoding for a VGA resolution image are shown in Table 1.

TABLE I. PROCESSING TIME OF DIFFERENT FUNCTIONS

Functions	Clocks	Execution Time
Sobel edge detector	5224652	8.36ms
JPEG compression	118284062	197ms

The maximal image acquisition rate is 100frame/s in VGA. With an on-board JPEG compression algorithm, the system can output frames in VGA resolution at 6 fps. Such frame rate is not fast enough for real-time video transmission. But for many embedded vision applications, it is not necessary to transfer the full captured images. The captured frames are supposed to be processed locally. Images of interest and high-level abstracted data are then transferred to the host computer via Ethernet interface. Such arrangement makes real-time embedded vision application possible.

The maximal power consumption of whole system is about 3w. Considering the fact that DM642 consumes 2Watt while running at 600MHz, the high power consumption rate of the imaging system is not surprising. An important task of our future work is to reduce the power consumption of the imaging system. For the present, what we do is turning off those unnecessary modules of DM642 to reduce power consumption. We plan to introduce the latest C64X processor (which has a same core to DM642 but consumes much less power) in the new version of imaging system.

V. CONCLUSION AND FUTURE WORK

This paper presents the design and implementation of an integrated image acquisition and processing system based on DM642 and a mega-pixel CMOS Image sensor. The system can be applied in intelligent video surveillance system, autonomous robots, and other embedded vision applications. By exploring the features of DM64X DSP processor and the CMOS image sensor, the system achieves the goal of integration of image acquisition and processing functions. Next, we will concentrate on the realization of more middle-level image processing functions, and on the improvement of on-board pre-processing functions.

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