

Developing a Dual-Stage Indirect Virtual Metrology Architecture

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ABSTRACT -- Over the past few years, the virtual metrology (VM) technology has been proposed and developed and several VM related papers have been published. These proposed VM architectures are mainly applied for conjecturing single-stage or direct processing quality. However, the processing quality of some of manufacturing processes cannot be measured directly. Those single-stage VM architectures may not be applied to handle this indirect VM problem accurately. To properly handle this indirect VM problem, the paper proposes a dual-stage indirect VM architecture (DIVMA), which involves two process tools, to handle the indirect VM problem. In Stage I, the direct VM model of the fore-tool is established as usual, and then the indirect VM model of the rear-tool is built in Stage II that involves the Stage-I VM output. The concept of virtual cassette is also proposed in the paper. The chemical vapor deposition (CVD) process of a fifth generation TFT-LCD fab in Chi Mei Optoelectronics Corporation (CMO), Taiwan is adopted to test and compare the conjecture accuracy without and with the virtual cassette and the proposed DIVMA. Experimental results demonstrate that the virtual-cassette concept is valid for improving VM conjecturing accuracy; also this DIVMA is adequate for handling the indirect VM problem that has a coupling effect between those two subsequent tools.

Index Terms -- Virtual metrology (VM), virtual cassette, indirect VM problem, dual-stage indirect VM architecture (DIVMA).

1. Introduction

Semiconductor and thin film transistor-liquid crystal display (TFT-LCD) are two high-capital and technology-intensive industries with leading roles in global hi-tech development for recent years. In these two hi-tech industries, on-line quality monitoring to each wafer/glass is required to ensure process stability and improve yield rate. However, it is very time-consuming and expensive if the actual metrology values of each wafer/glass are obtained by actual measurement. A feasible alternative is to apply virtual metrology (VM) technology [1], [2]. VM can be utilized to conjecture

wafer/glass quality based on the process data collected from production equipment when actual metrology is unavailable.

VM technique and many VM-related studies have been proposed recently. For example, Monahan [3] proposed the need for the transition from actual metrology to VM for enabling design for manufacturability (DFM) and advanced process control (APC) at the 32nm technology node. Chen et al. [4] suggested applying VM to enable wafer-to-wafer (W2W) control without additional actual metrology. Su et al. [5], [6] proposed a processing quality prognostics scheme (QPS) for plasma sputtering in TFT-LCD manufacturing. Chang et al. [7] utilized a piecewise linear neural network and a fuzzy neural network to design a VM architecture. Hung et al. [8] applied radial basis function networks (RBFN) to develop a VM architecture for predicting chemical-vapor-deposition (CVD) thickness in semiconductor manufacturing. Khan et al. published twin papers ([9] & [10]) to develop a distributed VM architecture for fab-wide VM and feedback control of semiconductor manufacturing processes using recursive partial least squares (PLS).

The VM architectures of those papers mentioned above are suitable only for solving the single-stage direct VM problem whose real metrology values (for training or tuning purposes) can be measured directly from the metrology tool. However, in some manufacturing processes, the process quality cannot be measured directly. Those single-stage VM architectures may not be applied to handle this indirect VM problem accurately. This paper proposes a dual-stage indirect VM architecture (DIVMA), which involves two process tools, to handle the indirect VM problem. In Stage I, the direct VM model of the fore-tool is established as usual, and then the indirect VM model of the rear-tool is built in Stage II that involves the Stage-I VM output.

As shown in Fig. 1, the dual-phase VM scheme [11] previously proposed by the authors is adopted as the basic tool to develop the DIVMA. The dual-phase VM scheme has the properties of considering both promptness and accuracy of the VM outputs and solving the on-line learning problem of VM. This dual-phase VM scheme also generates the VM accompanying reliance index (RI) and global similarity index (GSI) [12]. The RI and GSI are applied to gauge the reliance level of the VM conjecture values. If the reliance level of a VM value is lower than its threshold, this VM conjecture result may not be adopted. The inputs of the dual-phase VM scheme include process data of the current tool and pre-metrology

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(Pre-Y) data of the previous tool [13] as well as the

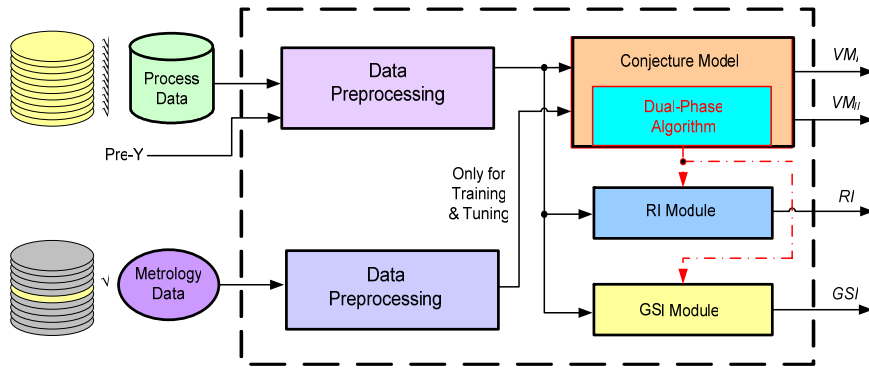


Fig. 1. Dual-Phase VM Scheme.

metrology data of the current tool. The Pre-Y data is also called Type-2 data in [9] and [10] and may be either actual or virtual metrology data. It is noted that the Pre-Y is treated as one of the process input data, whereas the Stage-I VM output of the DIVMA is considered in the Stage-II metrology input data that will be explained in Section 4.

The concept of virtual cassette is also proposed in the paper to improve VM conjecturing accuracy of TFT-LCD manufacturing. The CVD process of a fifth generation TFT-LCD factory in CMO, Taiwan is used as the illustrative example to test and verify the DIVMA accuracy. The remainder of this paper is organized as follows. The concept of a virtual cassette for handling TFT-LCD VM conjecturing is proposed in Section 2. Section 3 describes the indirect VM problem. Section 4 then presents the system architecture of the DIVMA. The experimental results are detailed in Section 5. Finally, a summary and conclusion are made in Section 6.

2. The Concept of a Virtual Cassette

For TFT-LCD manufacturing, each cassette contains 30 pieces of glass (also called glasspieces). Each CVD tool may contains five or six chambers. For reducing cycle time, after a cassette arrives at a tool station, all the glasspieces in the same cassette will be unloaded one by one and sent to each available chamber of the same tool randomly. Those after-process glasspieces will be loaded into a new cassette in a first-come-first-serve fashion. Consequently, each cassette contains glasspieces that are processed from various chambers. Generally, one out of 20 cassettes is chosen to select five or six glasspieces (one for each chamber) as the metrology glasspieces for quality monitoring. In summary, for a tool with five/six chambers, one out of 120/100 glasspieces is chosen as a metrology glasspiece for a specific chamber. Based upon the fact mentioned above and for obtaining an acceptable conjecturing accuracy, we cannot apply a single VM model (created and dedicated to the same chamber) to conjecture the VM values of all the glasspieces in the same real cassette because most of the glasspieces are not processed by the same chamber that creates the VM model. To resolve the problem mentioned above, the concept of a virtual cassette is proposed.

A virtual cassette is defined to contain many process glasspieces and one metrology glasspiece; those process and metrology glasspieces are processed by the same chamber. Moreover, a virtual cassette starts collecting process glasspieces that are processed by a specific chamber one by one and ends collecting until a metrology glasspiece of that same chamber has been obtained. This virtual-cassette concept can be realized by software. By applying the

virtual cassette, the dual-phase VM scheme [11] works perfectly for TFT-LCD manufacturing.

For semiconductor manufacturing, each cassette (also called FOUP) contains 25 wafers and, in general, each tool has multiple chambers and usually is not more than six. These multiple chambers also have different physical characteristics and operate independently. In a case, all the wafers in the same cassette are processed in the same chamber of a manufacturing tool. For some other cases, all the wafers are processed equally by multiple chambers. As a result, the wafers in the same chamber can apply the same VM model (created and dedicated to the same chamber) for VM conjecturing. In general, one of the wafers in the same chamber is selected as a real-measuring sample for quality monitoring. This real-measuring sample is denoted as a metrology wafer. The other wafers are called process wafers. Therefore, the dual-phase VM scheme [11] can also be applied to the semiconductor industry when the concept of virtual cassette is applied.

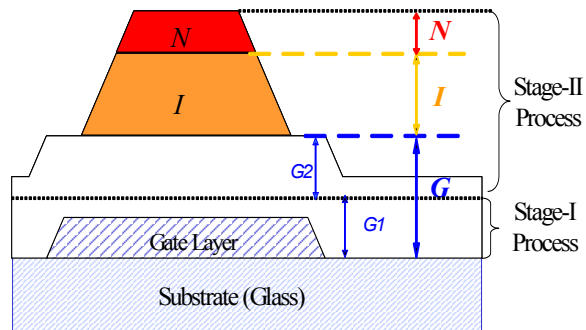


Fig. 2. Thin Film Structure in CVD Process.

3. The Indirect VM Problem

The CVD process in this study is to deposit three layers of different thin films (G, I, and N layers) on the substrate (Fig. 2). The G layer, gate insulator, comprises silane, ammonia and nitrogen. The I layer, intrinsic amorphous silicon, is formed via the CVD reaction between silane and hydrogen. The N layer, n-plus amorphous silicon, is deposited with silane, hydrogen, and phosphine. The G layer is decomposed into G1 and G2 ones to enhance the production yield. The G1 layer is plated in Stage-I

process, whereas the G2, I, and N layers are deposited in Stage-II process. The I and N layers are deposited on a single step, their quality monitorings of thickness can be performed by applying the regular VM conjecturing scheme. This study is focused on the quality monitoring of G1 and G2 thicknesses. The straightforward way of quality monitoring is to measure the G1 and G2 thicknesses directly. However, due to the physical constraint of the nanometer measurement tool (NANO), only G1 and G thicknesses are measured during Stage I and Stage II, respectively. As a result, G2 can merely be indirectly deduced by

$$G2 = G - G1 \quad (1)$$

As mentioned in Section 2, for a tool with five/six chambers, one out of 120/100 glasspieces is chosen as a metrology glasspiece for a specific chamber. A typical example shows that Stage-I tool has five chambers while Stage-II tool has six chambers. For this example, the

upper portion of Fig. 3, can be utilized. The concept of a virtual cassette is applied in VM_{G1} . All of the process glasspieces in the same virtual cassette are sent to the VM_{G1} for conjecturing the G1 layer VM values, denoted $\hat{G}1$. The metrology glasspiece, measured by the NANO, of the same virtual cassette is also sent to the VM_{G1} for re-training or tuning the G1 VM model. RI of Stage I ($RI_{\hat{G}1}$) and GSI of Stage I ($GSI_{\hat{G}1}$) are also shown in the upper portion of Fig. 3.

Stage II (VM_{G2})

The purpose of VM_{G2} is for conjecturing G2. However, G2 cannot be measured directly and G2 can only be deduced by Eq. (1). Moreover, because the chance for straight use of Eq. (1) (with real measurements of G and G1 on the same metrology glasspiece) is only 1/12000, the indirect VM_{G2} scheme with

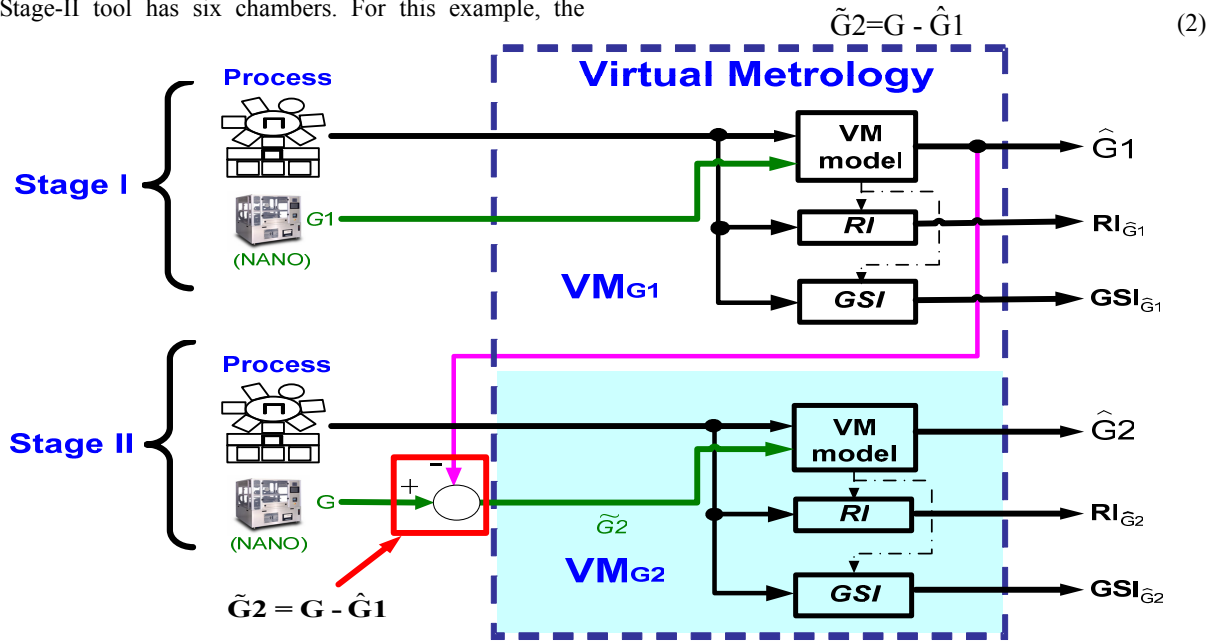


Fig. 3. Dual-stage Indirect VM Architecture (DIVMA).

chance of a specific glasspiece to have both G1 and G2 thicknesses been measured is only $(1/120) \times (1/100) = 1/12000$. Because the chance is so slim, it becomes clear about the reason why the DIVMA is required to accomplish the mission of monitoring the quality of G1 and G2 thicknesses for every individual glasspiece.

4. The Dual-stage Indirect VM Architecture

The DIVMA is illustrated in Fig. 3. Two dual-phase schemes (VM_{G1} for Stage I and VM_{G2} for Stage II) are applied in the DIVMA. VM_{G1} and VM_{G2} take care of G1 and G2 layers conjecturing, respectively. For the sake of simplicity, the blocks of data preprocessing and the Phase-II VM output of the dual-phase scheme (Fig. 1) are hidden.

Stage I (VM_{G1})

Because G1 can be measured directly, the conventional single-stage direct VM scheme (VM_{G1}), as shown in the

as shown in the red-square of Fig. 3 is proposed. Observing Eq. (2), $\tilde{G}2$ represents the synthesized G2 and $\hat{G}1$ is the G1 VM value (Stage I output) which is available as far as VM_{G1} functions normally. Again, applying the concept of a virtual cassette and feeding the process data of the process glasspieces of the Stage II tool, which deposits the G2 layer, and $\tilde{G}2$ of the metrology glasspiece to VM_{G2} , the G2 VM value, $\hat{G}2$, and its accompany RI/GSI values, $RI_{\hat{G}2} / GSI_{\hat{G}2}$, can be obtained.

5. Illustrative Examples

Two examples are presented in this paper, one for conjecturing $\hat{G}1$ and the other for $\hat{G}2$. All the experimental data were collected from CVD tools that are practically operating in a fifth generation TFT-LCD factory of CMO in Taiwan. A Stage-I CVD tool contains five chambers while a Stage-II CVD tool possesses six chambers. Both in Stages I and II, to assure the processing quality, 19

positions are measured on a 26"-product glasspiece. Due to space limitation, only the position 10 of those VM values is chosen for demonstration in this paper.

designated algorithms for creating the VM conjecture models. The conjecture accuracy measured by the test data was quantified by the mean absolute percentage error

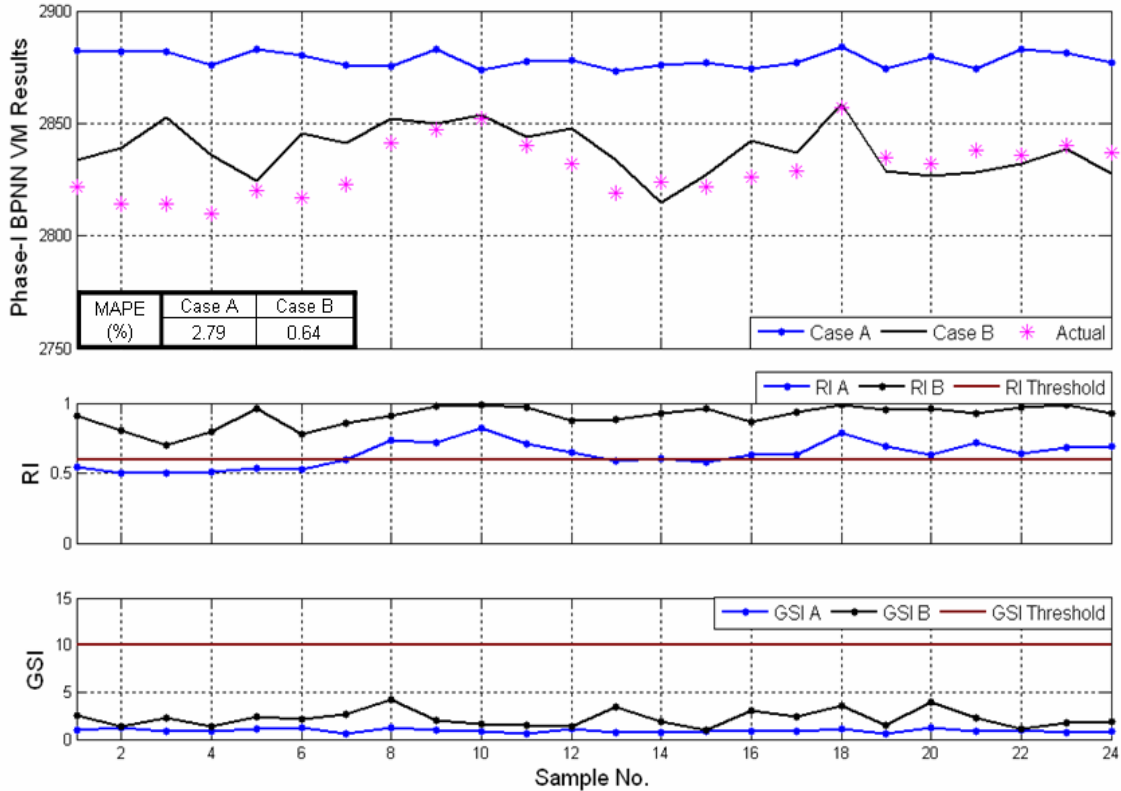


Fig. 4. Phase-I BPNN VM Results of G1 for Cases A and B at Position 10.

5.1 Example 1: G1 Conjecturing

Two cases are included in Example 1. Case A merges all the process and metrology glasspieces of all the five chambers in the same tool together to generate a common G1 VM model. The Case A G1 VM value is denoted by $\hat{G1}_M$. Case B applies the concept of virtual cassette. Therefore, each chamber has its own G1 VM model. The Case B G1 VM value is represented by $\hat{G1}$.

Case A involves 47+24 sets of process and the corresponding metrology sample data. The first 47 sets of sample data are mixed and collected from all of the five chambers. Those 47 sets of sample data are adopted for building the G1 VM model. The last 24 sets of sample data are collected merely from Chamber A. These 24 sets of sample data are applied for evaluating the G1 VM conjecturing accuracy.

Case B also includes 47+24 sets of sample data. However, because the concept of virtual cassette is enforced, the first 47 modeling sample data are all collected from Chamber A. As for the last 24 sets (for evaluating the conjecturing accuracy), they are the same as those 24 sets of Case A for equitable comparison.

According to the physical properties of a CVD tool and the experience of tool engineers, 10 significant process parameters are chosen as the inputs to the VM conjecture model. Back-propagation neural networks (BPNN) and multiple regression (MR) are adopted, in this study, as the

(MAPE) [5], [6], [11], [14]. The MAPE formula is shown as follows.

$$MAPE = \frac{\sum_{i=1}^n |(\hat{y}_i - y_i) / y_i|}{n} \times 100\% \quad (3)$$

where \hat{y}_i is the conjecture value, y_i is the actual metrology value, y is the target value, and n is the sample size. The closer MAPE values are to zero, the better the conjecture accuracy of the model can achieve. MAPE represents the average conjecture error of VM.

Among all the 19 measurement positions, the Phase-I BPNN VM conjecturing results of G1 at Position 10 is illustrated in Fig. 4. The MAPEs of Position 10 (2.79% vs. 0.64%) for Case A vs. Case B is shown in Fig. 4, respectively. Apparently, the conjecture accuracy at Positions 10 of Case B is much better than those of Case A.

As VM is practically applied, no actual metrology value can be utilized for evaluating conjecture accuracy. Thus, the VM conjecture value needs an accompanying RI and GSI to evaluate its reliance level and the GSI is to assist the RI in gauging the reliance level and locating the key parameter(s) that cause major deviation. The RI and GSI were proposed by the author [12] to gauge the degree of reliance. If the reliance index of a VM value is lower

than the threshold, this VM value may not be adopted [12].

By comparing the results shown in Fig. 4, it demonstrates that the conjecture values of Case B (\hat{G}_1) are much closer than that (\hat{G}_{1M}) of Case A to the actual values. Besides, it also reveals that the RI values of Cases B are higher than its threshold and superior to those of Case A. Thus, the Case A's VM values (\hat{G}_{1M}) may not be adopted because their reliance level is low [12]. Moreover, the GSI values of Cases A and B are both lower than their thresholds. This indicates that no property drift/shift occurs in the manufacturing process.

Case 1 utilizes \hat{G}_{1M} of Case A (defined in Example 1) to calculate the synthesized G_2 , \tilde{G}_{2M} :

$$\tilde{G}_{2M} = G - \hat{G}_{1M} \quad (4)$$

Case 2 applies \hat{G}_1 of Case B (defined in Example 1) and Eq. (2) to compute the synthesized G_2 , \tilde{G}_2 . Finally, Case 3 follows Eq. (1) to calculate G_2 by special arrangements to directly measure the G and G_1 values on the same metrology glasspiece. The purpose of Case 3 is to obtain the best possible conjecturing accuracy of G_2 .

Among all the 19 measurement positions for the CVD

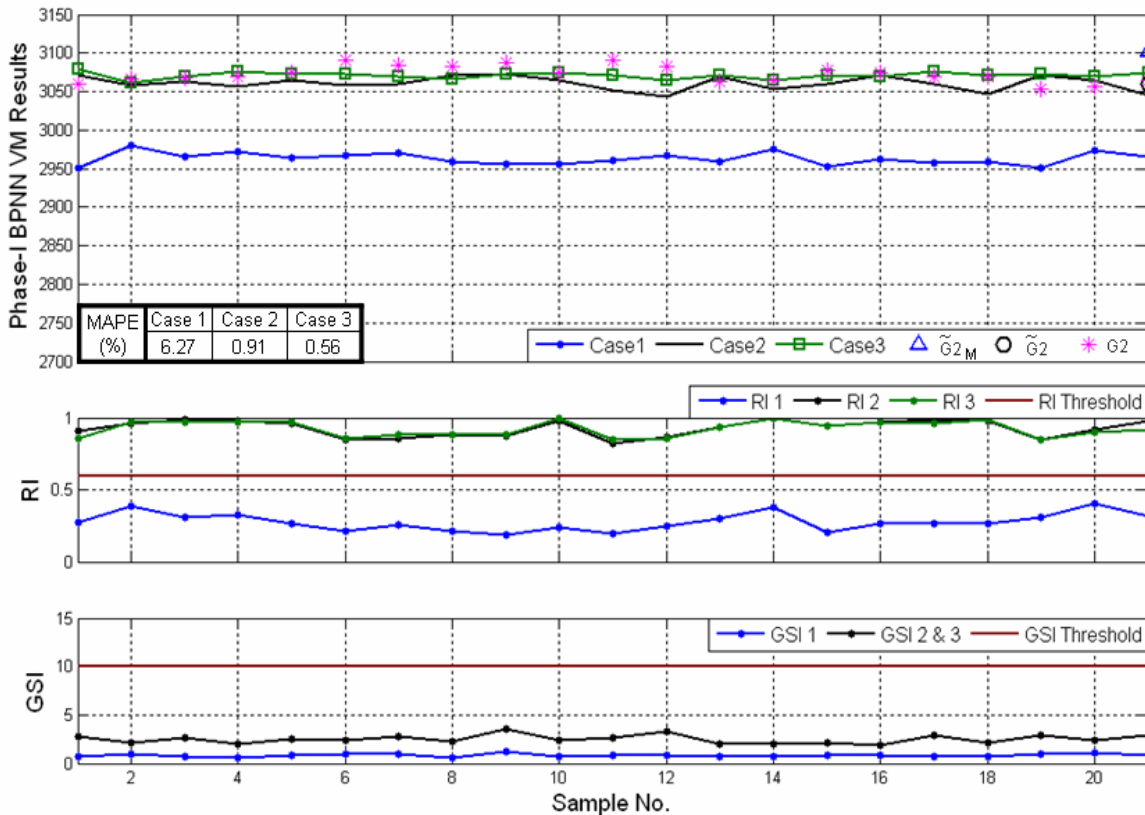


Fig. 5. Phase-I BPNN VM Results of G2 Cases 1~3 at Position 10.

5.2 Example 2: G2 Conjecturing

Example 2 contains three cases. Cases 1, 2, and 3 all encompass 23+21 sets of sample data. The first 23 sets of Case 1 sample data are mixed and collected from all of the six chambers of a Stage-II tool. Those 23 sets of sample data are adopted for building the G_2 VM model. The last 21 sets of sample data are collected merely from Chamber A. These 21 sets of sample data are applied for evaluating the G_2 VM conjecturing accuracy.

By enforcing the concept of virtual cassette, all the 23+21 sample data of Cases 2 and 3 are all collected from Chamber A of a Stage-II tool. Those first 23 sets of sample data are adopted for building the G_2 VM model. The last 21 sets of sample data are the same as those of Case 1 and applied for evaluating the G_2 VM conjecturing accuracy.

process of 26''-product glass, the Phase-I BPNN VM results of G_2 at Position 10 is illustrated in Fig. 5. Observing Fig. 5, each test sample has a real-measurement $G_2 (= G - G_1)$ value for evaluating its VM conjecturing accuracy. Only Sample no. 21 has \tilde{G}_{2M} , G_2 , and \tilde{G}_2 values for accuracy comparison. It appears that the values of \tilde{G}_2 and G_2 are about the same while that of \tilde{G}_{2M} are somewhat different from G_2 . Because G_2 value is the main reference of VM, this observation can deduce that Case 3's conjecturing result should have the best accuracy, Case 2's result will be about the same as that of Case 3, and Case 1's result won't be accurate enough. This deduction is verified by checking the MAPEs of Cases 3, 2, and 1; they are 0.56%, 0.91%, and 6.27%, respectively. Note that, besides \tilde{G}_{2M} , the cause of large MAPE of Case 1 is partly due to the fact that Case 1's modeling sample data are mixed and collected from all

of the six chambers. The RI curves on Fig. 5 also reveal that Case 1's RI values are much smaller than those of Cases 2 and 3. Low RI value implies that its corresponding VM value has low reliance. Therefore, Case 1's VM conjecturing results are less reliable. Moreover, no property drift/shift occurs in the manufacturing processes of all the three cases because the GSI values of Cases 1, 2, and 3 are all lower than their thresholds.

6. Summary and Conclusions

This paper proposes a dual-stage indirect VM architecture (DIVMA), which involves two process tools, to handle the indirect VM problem. In Stage I, the direct VM model of the fore-tool is established as usual, and then the indirect VM model of the rear-tool is built in Stage II that involves the Stage-I VM output. The concept of virtual cassette is also proposed in the paper. The feasibility of DIVMA with virtual cassette (Case 2) is verified by an illustrated example. The concept of virtual cassette and DIVMA has been successfully deployed in a fifth-generation TFT-LCD fab in Taiwan.

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