Analysis of the Dynamic Oscillatory Process of a Neural-type Cell (NTC) and Its Input Voltage Bounds

Zhengqing Wu
Department of Electrical Engineering
Xi'an Jiaotong University
Xi'an, Shaanxi, 710049, China
Email: wzq201101@stu.xjtu.edu.cn

Robert W. Newcomb
Department of Electrical and Computer Engineering
University of Maryland
College Park, MD, 20742, USA
Email: newcomb@eng.umd.edu

Abstract—A neural-type cell (NTC) is an electronic circuit that mimics the behavior of a neuron. This paper mainly focuses on one type of NTC. It oscillates to produce pulse-coded signals. A complete description of the NTC's oscillation is offered in this paper. The description takes the body effect into consideration, which was never included in previous research work. Moreover, before, it was noticed by researchers that the NTC was able to oscillate only when the input voltage is within a certain range. However, an explanation of the physical essence of the input bounds has yet to be found. To tackle this, this paper provides detailed analysis to the turn-on/off input voltages. Additionally, although there has been a method proposed to calculate the input voltage bounds of an older version of NTC, it was based on numerical approximation and thus lacked universality. In this paper, a new way of calculating the oscillation-supporting input range for the latest version of NTC, the all-MOS NTC, is put forward.

Keywords—NTC, neural-type cell, pulse-coded, oscillation, input range, hysteresis, artificial neuron model, spiking neural network

I. INTRODUCTION

The term, neural-type cell (NTC), was first coined by Dr. Nick Declaris while conducting a Polish-USA study into neural-type microsystems in the 1970s [1]. The neural-type cell (NTC) was invented to imitate the behavior of neurons. One way of doing this is to realize the Hodgkin-Huxley equations [2] with electronic devices, which might involve a complex circuit when implemented in silicon. One other form of NTC was invented later to bypass the intricacy of the Hodgkin-Huxley equations and can be realized with a much simpler circuit. Kuklarni-Kohli and R. W. Newcomb's work [3] contributed to an NTC of this
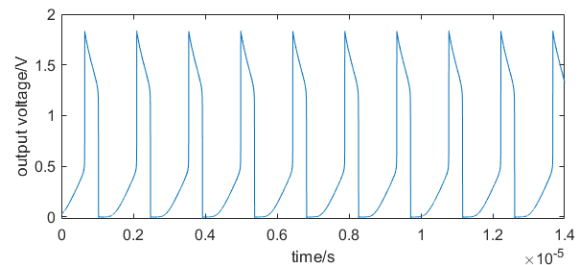

Fig. 1 The pulse-coded signals produced by the NTC

kind. The basic unit of this NTC was presented in [4], and a detailed analysis of the mechanism of this circuit was also offered in that paper. In short, the NTC oscillates to produce pulse-coded signals, which is shown in Fig. 1. The oscillation of the circuit is mainly resulted by the intersections of the load curve and the output characteristic curve (a hysteresis) at the latter's steep edges, causing the circuit to stay unstable. Reference [4] also enlarged on the hysteretic property of the NTC by bringing up a mathematical description of the hysteresis. The oscillation could also be supported with the semistate theory [5].

Moreover, it was noticed that the oscillation of an NTC could only happen when its input voltage is within a certain range. This phenomenon was revealed in [6], and a method of calculating the input voltage range was presented in that paper. However, the calculation is merely based on a numerical approximation without taking the actual physical process into account, which made this method lack universality.
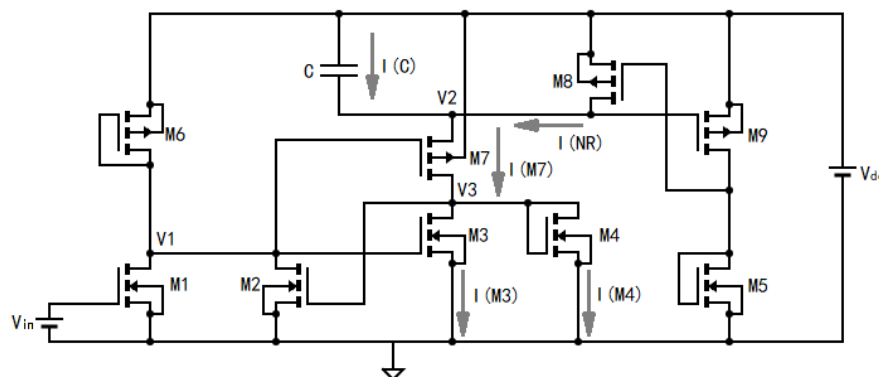

Fig. 2 A circuit diagram of the NTC

In all the research mentioned above, the NTC unit was composed of both MOSFETs and resistors. According to [7], such NTC might incur several limitations including a comparatively large size and a small range of input voltage to support oscillation. So, reference [7] provided an improved version of NTC – the all-MOS NTC (shown in Fig. 2), solving the two limitations listed above. The modification involved changes in both the load curve and the output characteristic curve of the NTC, but the principle of oscillation remained unaltered. The output characteristic curve and the load curve of an all-MOS NTC can be seen in Fig. 8. The meanings of the variables in Fig. 8 are shown in Fig. 2.

Several applications involving the NTC unit have also been proposed. For example, by cooperating with the Hartline pools, which can help to integrate voltage, the NTC unit can realize some biological functions of neurons [8]; reference [9] specifies another method to perform synaptic weighting and summation using the NTC; moreover, connecting a series of NTCs to each other in a head-to-tail manner can build a neuristor line [3]; besides, to build up necessary components for pulse-coded neural networks, a complete scheme is put forward in [10]; furthermore, the NTC units also support the synchronization of spikes and produce chaotic signals [11] [12]; other than these, researchers have also attempted to realize several Boolean functions with the NTC [13].

Nevertheless, several problems about the NTC still await solutions: 1) A complete description for the process of its oscillation is missing; 2) The explanation for why the oscillation-supporting input voltage bounds exists remains unclear; 3) Because of the lack of understanding of the actual oscillatory behavior, the already-existing method to calculate the input voltage bounds, which is for the earlier version of NTC, is inaccurate; more importantly, there hasn't been any attempt for a method to calculate the input voltage bounds for the more useful all-MOS NTC, which was invented later. These problems will be tackled in this paper.

II. ANALYSIS OF THE DYNAMIC PROCESS OF THE NTC

Most of the previous work in this field analyzed the NTC by taking advantage of the hysteresis curve. However, due to the extreme nonlinearity of the circuit, the mathematical description [4] of this hysteresis is based on ideal assumptions. This way of description is sufficient for demonstrating the existence of the hysteresis, but not accurate enough to quantify the status of the circuit; also, how the circuit transits between status was never well described before. Thus, the actual physical process should be focused on here. To make it easier for demonstration, an all-MOS NTC composed of 180nm MOSFETs is used for simulation (shown in Fig. 2).

The parameters for the devices used in this circuit unit are: $W_1 = 7.8\mu m$, $L_1 = 1.3\mu m$, $W_2 = 13\mu m$, $L_2 = 1.3\mu m$, $W_3 = 1.6\mu m$, $L_3 = 1.6\mu m$, $W_4 = 3.9um$, $L_4 = 1.3\mu m$, $W_5 = 1.6\mu m$, $L_5 = 1.6\mu m$, $W_6 = 14.3\mu m$, $L_6 = 1.3\mu m$, $W_7 = 26\mu m$, $L_7 = 1.3\mu m$, $W_8 = 2.6\mu m$, $L_8 = 1.3\mu m$, $W_9 = 2.6\mu m$, $L_9 = 1.3\mu m$, $k_p' = 32.95\mu A/V^2$, $k_n' = 134.00\mu A/V^2$, $V_{tn} = 0.3545V$, $V_{tp} = 0.4121V$, $V_{dd} = 3V$. L_i and W_i stand for the length and width of the MOSFET with a subscript of i; k_p' and k_n' stand for the process transconductance parameters [14] of PMOS and NMOS; and V_{tp}, V_{tn} refers to the threshold voltage of PMOS and NMOS without body effect. All

the threshold voltages in this paper are treated as positive numbers. The capacitor in this circuit unit need not have a fixed value. Different capacitance can yield different oscillatory frequencies. With experiments, a recommended range of the value of the capacitance is established as 20pF~1mF.

A brief description of the oscillating circuit was provided in [12]. However, the change of the threshold voltage of M_7 due to its body effect was not mentioned in that paper. It will be shown in the next part of this paper that the body effect plays an indispensable role in the oscillation cycle. Hence, part of the process of the oscillation was not fully discussed in [12].

For convenience of explanation, the circuit in Fig.2 is separated into several parts: 1) the input branch (M_1, M_2, and M_6); 2) the output branch (M_7, M_3, and M_4); 3) the nonlinear resistor [7] (M_5, M_8, and M_9). The input is defined to be the gate-to-source voltage of M_1, and the output is defined as V_3, as is shown in Fig. 2. Usually, when making use of the NTC, V_3 is treated as the output voltage, and that is where the spiking signals (shown in Fig. 1) are produced. However, it is worth mentioning that the load curve and the hysteretic output characteristic curve, as are mentioned in the introduction part and reference [4], are based on the viewpoint which treats V_2 as an output and the nonlinear resister as a load.

With analysis of the simulation results, the principle of the entire process of NTC's oscillation can be extracted. A few waveforms that are important for the demonstration of the process are presented in Fig. 3(a)-(k).

Here below is an expatiation of the oscillation process:

There are two distinct phases in one cycle. The first phase (P_1) is when M_2 and M_4 are off, which means V_3 is less than V_{tn}, and the other one (P_2) refers to the opposite situation. The oscillation corresponds to the scenario that the circuit endlessly jumps from one phase to the other. The two phases are both marked in all of the waveforms in Fig. 3(a)-(k) to facilitate further explanation.

In P_1, since V_3 is quite low (Fig. 3(a)), M_2 only passes a tiny amount of current (Fig. 3(c)). The current through M_6, consequently, should also be smaller than in P_2 (Fig. 3(d)). (This is because the changing range of the M_1's current is very small (Fig. 3(b)). In fact, M_1 was initially designed to function as a current source [4].) Thus, the voltage drop across the diode-connected M_6 should also be smaller. V_1, as a result, is kept at a higher level (Fig. 3(e)), close enough to V_{dd}, limiting the capability of M_7 to let-through current (Fig. 3(f)). The output branch is enduring a small amount of current, which means most of the current flowing from the nonlinear resistor (Fig. 3(g)) will pass through the capacitor from the lower end to the higher end in Fig.2, causing $I(C)$ to be negative in value (Fig. 3(c)). (A more detailed discussion about the current will be provided in the last part of this section.) This will cause V_2 to rise (Fig. 3(i)), lowering the absolute value of the voltage drop between the body and the source (V_{bs}) of M_7. The body effect of this transistor will be mitigated, and its threshold voltage will drop. At the same time, as the $V_{sg}(M_7)$ rises due to the increase of V_2, the output branch starts to inject an ascending amount of current through M_7.
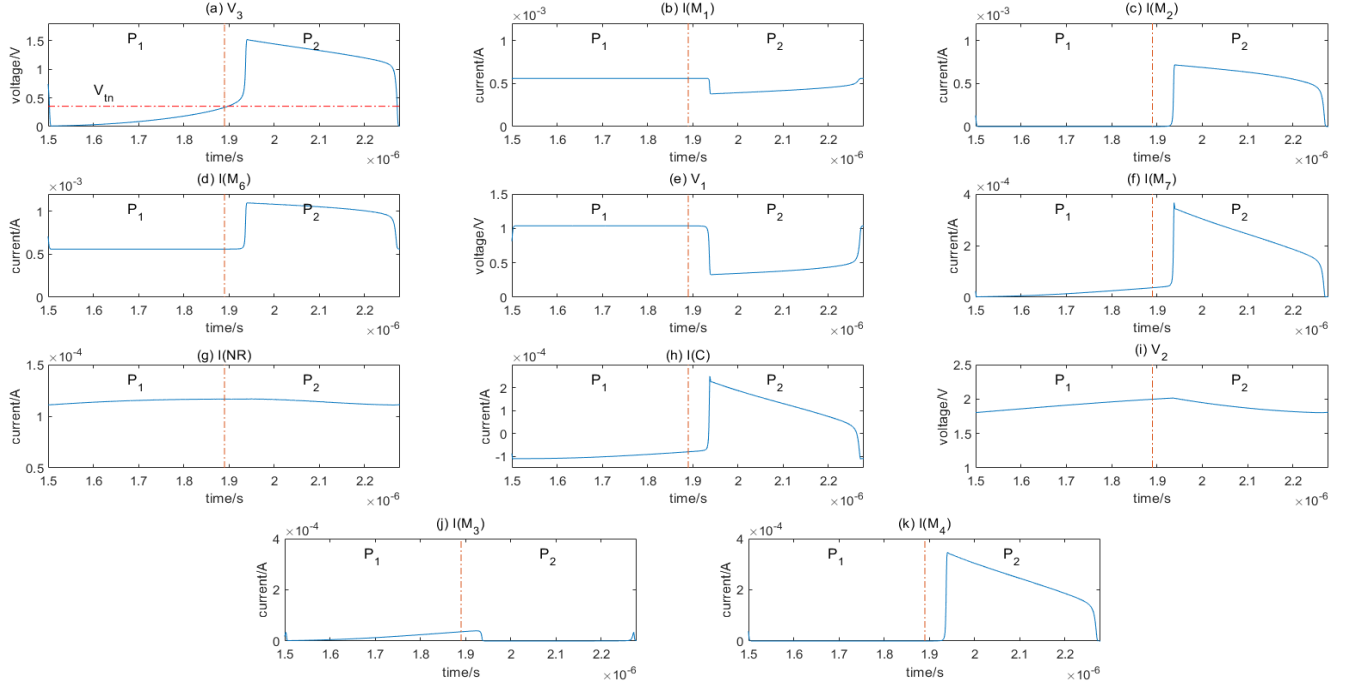
Fig. 3 A set of waveforms used to analyze the oscillation procedure of the NTC: All the waveforms are truncated to approximately one oscillation cycle and separated into P_1 (Phase 1) and P_2 (Phase 2).

As is mentioned, V_3, at this point, is lower than V_{tn}, which means it must be much lower than V_1, so M_3 is working in the triode region (Fig. 3(j)), while M_4 is off (Fig. 3(k)). This denotes that the current through the output branch mainly passes M_3. Meanwhile, the gate voltage of M_3, V_1, stays stable in this phase. So, when the current through the output branch increases, the drain-to-source voltage of M_3 will be raised. The moment that V_{ds} of M_3, which is also the V_{gs} of M_2 and M_4, exceeds V_{tn} marks the NTC entering P_2.

In the early stage of P_2, as M_2 is turned on to take in a large amount of current, the current through M_6 increases accordingly, bringing down V_1. As a result, the V_{sg} of M_7 increases to enable this transistor to pass an increasing amount of current; on the other hand, the V_{gs} of M_3 drops, and M_3 refuses to absorb large current. These two factors force diode-connected M_4 to soak in large current, further pumping up V_3 from V_{tn}. Then the current through M_2 gets increased again, bringing down V_1 … This process can account for the steep edges in the waveforms of Fig. 3(a)-(f), (h), (j), (k) when the circuit just enters in P_2. The NTC keeps moving on with this tendency until next a few things happen.

Since $V_{sg}(M_7)$ is growing in P_2 up till this stage, the current through M_7 is also increasing. The current provided by the nonlinear resistor then switches its way from the capacitor to the output branch. However, the output branch is asking for more current than the nonlinear resistor can offer. Consequently, instead of continuing taking in current from the nonlinear resistor, the capacitor needs to give out current to the output branch. The current of the capacitor starts to flow from the upper end to the lower end, charging the capacitor, lowering V_2. The source-to-body voltage of M_7 will increase accordingly,

and it intensifies the body effect of M_7. The resultant increase of its threshold voltage will limit its capability to let-through large current. The tendency mentioned in the previous paragraph is curbed and reversed. At the end of P_2, the current through the output branch is a very small value, which makes the voltage drop across M_3 and M_4 no longer able to support M_2 and M_4 to be on. The NTC will now transit into P_1. A full cycle of the oscillation is completed.

There is one critical detail of the oscillation remaining undiscussed, mainly concerning the changing process of the current through the output branch: what if the current provided by the nonlinear resistor is little when the current demand of the output branch is little (in P_1) and large in the opposite situation? If it were the case, there would not be enough fluctuation of current through the capacitor to change the source-to-body voltage of M_7 then. However, in fact, there is no such worry. The difference of current needed by the output branch in different phases transcends the difference of the current from the nonlinear resistor in different phases. Thus, large current fluctuation of the capacitor is needed to make up the current demanded by the output branch in the early stage of P_2, which supports the change of the body effect.

To provide a clearer overview of the oscillation cycle, a cycle diagram is provided in Fig. 4. To cut the long story short, the body effect and the comparative relationship between V_3 and $V_{th}(M_2)$ are the two critical factors of the dynamic behavior of this NTC.

III. ANALYSIS OF THE LOWER AND UPPER BOUNDS OF NTC'S INPUT VOLTAGE AND THEIR CALCULATIONS
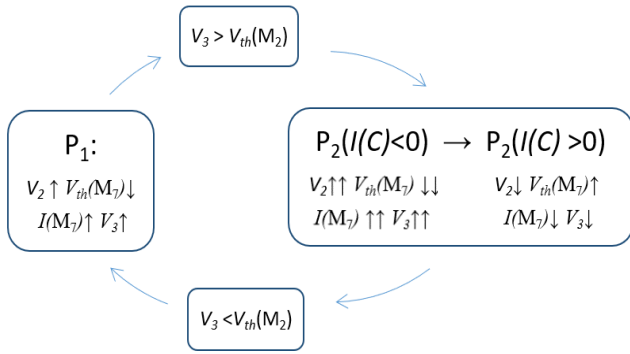
Fig. 4 A cycle diagram of the oscillation process: double arrows like ↑↑ and ↓↓ mean the value is changing drastically

Fig. 5 The change of the output signal (V_3) when the input voltage steps across the lower bound

With the aforementioned analysis of the actual process of the oscillation, the analysis and calculation of the lower bound ($V_{in,low}$) and upper bound ($V_{in,high}$) of the input voltage of the NTC are ready to be presented. The NTC can oscillate only within this range. This part will shed light on the physical meanings of both of the input voltage bounds followed by the methods to calculate them. The causes of the inaccuracy of the calculation results are also investigated. The analysis of the lower and upper bound will be addressed separately.

A. The Analysis and Calculation of the Lower Bound

The output of the NTC as the input voltage increases from 0V is shown in Fig. 5.

Fig. 5 is a simulation of V_3 using a ramp voltage source which sweeps from 0 to 1.4V as the input of the NTC. As is shown in Fig. 5, when V_{in} is around 1.1V, the circuit starts to oscillate. This is approximately when V_3 transcends V_{tn}, which turns on M_2 and M_4. The rapidly increasing current passing M_4 will raise the current though the output branch. The current will soon outweigh what can be provided by the nonlinear resistor, and this will activate the capacitor, which passes no current when the circuit is static. According to what is mentioned in the previous section, this will add dynamics to the system and trigger the oscillation. However, contribution merely from M_4 is not sufficient to support the start of oscillation. As M_4's current demand causing current to flow through the capacitor from the upper end to the lower end, V_2 is brought down consequently. This will limit M_7's capability to let-through current, and the current through the output branch will be decreased, which hold back the circuit from entering oscillatory status. M_2, on the other hand, prevents this from happening. As M_2 passes a large amount of current, V_1 is brought down, increasing $V_{sg}(M_7)$. Thus, although having its threshold voltage raised as a result of an increasing amount of current through M_4, M_7 is still able to pass an increasing amount of current owing to the rise of its source-to-gate voltage engendered by M_2. This is how the first spike in Fig. 5 is formulated.

With the analysis of the lower bound presented above, calculation of the $V_{in,low}$ can be presented in this part. The situation where V_{in} is just below $V_{in,low}$ is focused on here. Since the NTC is still stable in this situation, there is no current flowing through the capacitor. Additionally, the current through M_4, $I(M_4)$, is negligible because it is not comparable to the current through M_3, $I(M_3)$. Thus, we can derive the equations
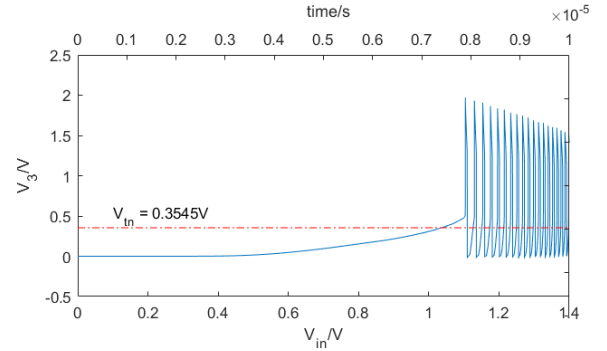
that we need: the current from the nonlinear resistor $I(NR)$ equals $I(M_7)$ and $I(M_3)$.

First, $I(NR)$ is calculated. Because $I(M_5)$ must be the same as $I(M_9)$, we have:

$$\frac{1}{2}k_p'\left(\frac{W_9}{L_9}\right)\left(V_{dd}-V_2-V_{tp}\right)^2 = \frac{1}{2}k_n'\left(\frac{W_5}{L_5}\right)\left(V_{g8}-V_{tn}\right)^2 \quad (1)$$

V_{g8} is the gate voltage of M_8, which is also the drain-to-source voltage of M_5. After a reorganization of (1), we can get that V_{g8} is a linear function of V_2:

$$V_{g8} = V_{tn} + \sqrt{\frac{k_p'}{k_n'}\left(\frac{W_9 L_5}{W_5 L_9}\right)}\left(V_{dd}-V_2-V_{tp}\right) = V_{g8}(V_2) \quad (2)$$

Suppose M_8 works in its triode region, $I(NR)$ will be:

$$I(NR) = I_{sd}(M_8) = k_p'\left(\frac{W_8}{L_8}\right)\left[\left(V_{dd}-V_{g8}-V_{tp}\right) - \frac{1}{2}(V_{dd}-V_2)\right](V_{dd}-V_2) \quad (3)$$

V_3 equals V_{tn} at this moment, so $V_{sd}(M_7)$ should be large enough to make M_7 work in the saturation region. Hence, $I(M_7)$ can be represented as:

$$I(M_7) = \frac{1}{2}k_p'\left(\frac{W_7}{L_7}\right)\left[V_2-V_1-V_{tp}(V_2)\right]^2 \quad (4)$$

Here, V_{tp} is a function of V_2 because of the body effect.

Since $V_g(M_3)$, namely V_1, is high, and $V_d(M_3)$ is as low as V_{tn}, M_3 can be inferred to be working in the triode region at this point. So, $I(M_3)$ is:

$$I(M_3) = k_n'\left(\frac{W_3}{L_3}\right)\left[(V_1-V_{tn})V_{tn}-\frac{1}{2}V_{tn}^2\right] \quad (5)$$

The left-hand sides of (3), (4) and (5) are the same value; a new variable is established to represent it -- I_{OB}. OB stands for "output branch".

(3), (4) and (5) altogether constitute a set of simultaneous equations with three unknown variables: V_2, V_1, and I_{OB}. Solving this equation set can yield the values of these variables. Then, we take V_1 into the next equation which indicates the

equality of the current through M_6 and M_1 when M_2 is off, which is the case when the NTC's input voltage is below the lower bound:

$$\frac{1}{2}k'_p\left(\frac{W_6}{L_6}\right)(V_{dd} - V_1 - V_{tp})^2 = \frac{1}{2}k'_n\left(\frac{W_1}{L_1}\right)(V_{in} - V_{tn})^2 \quad (6)$$

Equation (6) gives the solution of V_{in}, which is $V_{in,low}$.

Numerical Confirmation

The NTC configured using the data listed in Section II is taken as an example for numerical confirmation.

First, a function is required to describe the body effect (Fig. 6(a)). To simplify the calculation, a linear curve fitting (Fig. 6(b)) is adopted to reveal the relationship between the threshold voltage (V_{tp}) and the source-to-body voltage (V_{sb}). The function is:

$$V_{tp}(M_7) = 0.2709V_{bs} + 0.4255 \quad (7)$$

As is shown in Fig. 6(b), this linear function is accurate enough for the body effect of a PMOS of 180nm TSMC technology. The RMSE (root-mean-square error) is 0.0003373, and the R^2 (coefficient of determination) equals 0.996.

By solving (3), (4) and (5), we can get two sets of real solutions: $V_{2,1}$=2.6011V, $I_{OB,1}$=53.6910 µA, and $V_{1,1}$=1.6639 V; $V_{2,2}$= 2.2991V, $I_{OB,2}$=77.6132 µA, and $V_{1,2}$= 2.1690V. The second solution should be discarded because $V_{2,2}$ and $V_{1,2}$ are too close in this case, which means $V_{sg}(M_7)$ is too small for M_7 to provide current as large as $I_{OB,2}$. Taking $V_{1,1}$ into (6), the final solution for V_{in} can be given. The final result for $V_{in,low}$ is 0.9749V. According to PSpice simulation results, the actual
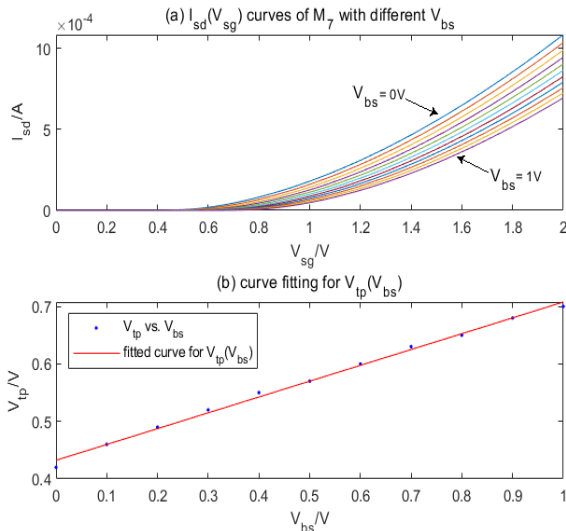

Fig. 6 (a) The existence of the body effect: This set of curves is obtained by running a parametric sweep simulation over V_{bs} (from 0V to 1V using 0.1V as an interval) and a DC sweep simulation over V_{sg} (from 0V to 1.9V). These curves (from left to right) each corresponds to different V_{bs} values (from low to high). (b) The curve fitting result of the V_{tp}-V_{bs} function: The curve fitting is performed using the curve fitting toolbox of MATLAB.

results are approximately: V_2 = 2.4346V, I_{OB} = 88.036 µA, V_1 = 1.4251V, and $V_{in,low}$= 1.1140V.

It can be noticed that, indeed, the calculation result deviates from the simulation result to some extent. There are mainly two reasons for that:

In the first place, the point that we define as the lower bound is not absolutely precise. In other words, when V_3 steps across V_{tn}, as M_2 and M_4 are just turned on, they still pass a small amount of current and cannot result in a dramatic change in the circuit. Fig. 5 also testifies to this: the circuit will start to oscillate slightly later than when V_3 reaches V_{tn}. From the figure we can measure the V_{in} at the intersection of V_{tn} and V_3, which is 1.0368V. Comparing the derived $V_{in,low}$ with this value, we can find the calculation method essentially possesses high precision. In practice, if a more accurate solution is required, one can replace the V_{tn} in (3) with a slightly larger value.

Secondly, the inaccuracy of the calculation is also caused by the fact that the formula we have for the current of a 180nm MOS working in the triode region is smaller than it actually should be. The analytical model that we used for calculation is different from the BSIM3 level 7 PSpice model that we used for simulation. This is reflected by the deviation of the calculated I_{OB} from the actual I_{OB} in simulation.

B. The Analysis and Calculation of the Upper Bound

Fig. 7 is an illustration of the change of oscillation of V_2 when the input voltage of the NTC increases. As is shown in this figure, the amplitude of the oscillation of V_2 will decrease. This is because the hysteretic output characteristic curve will shrink and its two intersections with the load line will get closer. Fig. 8 gives an illustration of this. The moment when the two intersections converge to each other is when the oscillation totally vanishes. V_{in} at this point is $V_{in,high}$.

To get $V_{in,high}$, it is necessary to describe the fading of the oscillation. Here is a way to achieve this: two status are specified within every single oscillation cycle, and the V_2 of these two status, $V_{2,status1}$ and $V_{2,status2}$, should be functions of only V_{in}. When the two curves of these two functions intersect, it means the two distinct status converge to one, signifying the amplitude of oscillation to be zero, thus the corresponding V_{in} denotes $V_{in,high}$.

The first status deserving attention can be depicted as follows. At the end of P_2, the body effect causes $V_{tp}(M_7)$ to be larger than $V_{sg}(M_7)$, limiting the amount of current passing through M_7. However, later, in P_1, as the capacitor discharges itself to a certain extent, there must be a moment when $V_{tp}(M_7)$ equals $V_{sg}(M_7)$ so that the output branch can pass increasing amount of current to transit the circuit back to P_2 again. This is the first moment to focus on. We have:

$$V_1 = V_2 - (k_1(V_{dd}-V_2) + k_2) \quad (8)$$

$(k_1(V_{dd}-V_2)+k_2)$ is a linear approximation of the function of $V_{tp}(V_2)$. It has been proved to be accurate enough.
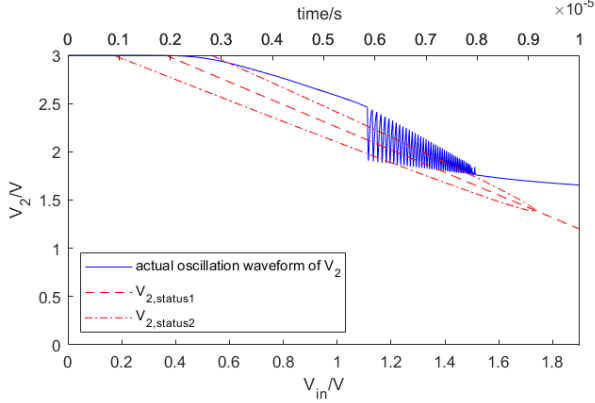
Fig. 7 The decreasing amplitude of V_2's oscillation when the input voltage increases: This simulation is done by connecting the NTC's input to a ramp voltage source which sweeps from 0 to 1.9V. The dash line and the dot dash line are respectively $V_{2,status1}(V_{in})$ and $V_{2,status2}(V_{in})$.

Equation (6) also holds for this moment because the moment focused on here belongs to P_1, during which M_2 is off. After a rearrangement of this equation, V_1 becomes a linear function of V_{in}:

$$V_1 = -\sqrt{\frac{k_n' W_1 L_6}{k_p' L_1 W_6}}(V_{in} - V_{tn}) + V_{dd} - V_{tp} \qquad (9)$$

When equaling the right hand sides of (8) and (9) to each other, the function $V_{2,status1}(V_{in})$ can be obtained:

$$V_2 = \frac{-\sqrt{\frac{k_n' W_1 L_6}{k_p' L_1 W_6}}(V_{in}-V_{tn})+V_{dd}-V_{tp}+k_2+k_1 V_{dd}}{1+k_1} = V_{2,status1} \qquad (10)$$

The second moment to focus on is: at the end of P_1, the current of the output branch increases to a level that makes V_3 equals V_{tn}. This scenario is very similar to the one focused on when calculating $V_{in,low}$, the only difference is that in this case, the current through the capacitor is not zero. But (4), (5) and (6) can still be made use of, so is (9), which is just another form of (6). Moreover, the current through M_7 and M_3 are still the same because the current through M_4 is ignorable in P_1.

Thus, it is reasonable to construct another equation out of (4) and (5) and replace the V_1 in both sides of the equation with a function of V_{in}, which is given in (9). So, the curve for $V_{2,status2}(V_{in})$ can result:

$$k_p'\left(\frac{W_3}{L_3}\right)\left((V_1(V_{in})-V_{tn})V_{tn}-\frac{1}{2}V_{tn}^2\right) =$$
$$\frac{1}{2}k_p'\left(\frac{W_7}{L_7}\right)\left(V_{2,status2}-V_1(V_{in})-V_{tp}(V_{2,status2})\right)^2 \quad (11)$$

When $V_{2,status1}$ equals $V_{2,status2}$, we can combine (10) and (11) to form a new equation, the only unknown variable being V_{in}. The solution of this equation is $V_{in,high}$. This equation, essentially, is just the same as replacing the right-hand side of (11) with zero. This is because (10) is depicting the scenario
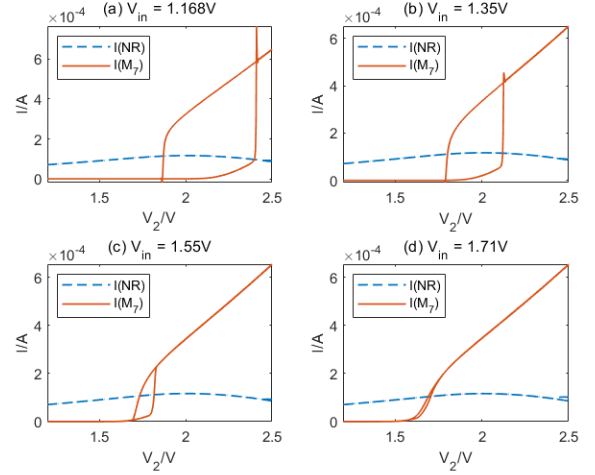

Fig. 8 The changing of the hysteresis' shape when the input voltage is increasing: To verify the hysteresis, a ramp voltage source is connected to the point where V_2 is marked in Fig. 2. The ramp is initiated at 0V, rises to 3V, then drops back to 0V over a time of 2ms.

when the source-to-gate voltage and the threshold voltage of M_7 are the same, so the calculated current through M_7 must be zero then, and the right-hand side of (11) is the formula for M_7's current.

Numerical Confirmation

The 180nm NTC in Fig. 2 is used again to verify the calculation method provided above. The curves for (10) and (11) are plotted together with the oscillation waveform in Fig. 7. The solution for $V_{in,high}$ is 1.71V, while the actual value is approximately 1.50V.

The model that is used here incurs inaccuracy when the input voltage is quite close to the higher bound. This is because the phase, P_1, which we select the two status from, does not exist in the strict sense when V_{in} is close to $V_{in,high}$. P_1 is defined as the moment when M_2 and M_4 are completely shut down. But, as P_1 and P_2 gets extremely close to each other, there will be no such moment because the simulation results reveal that V_3 will oscillate around or above V_{tn} when the input voltage is relatively high. In other words, P_1 and P_2 at this point are so close to each other that the actual oscillating status of the circuit should be deemed as a transitional point of these two phases; as a result, none of the characters of P_1 and P_2 can precisely describe this status. Furtherly, this will affect the precision of (10) and (11) because of the following reasons. (10) describes the moment when M_7 is just turned on, and its current is zero theoretically; However, since V_{tn} is oscillating at a high level, M_3 and M_4 will be passing current that cannot be neglected. Thus, the current of M_7, which should be the sum of the current through M_3 and M_4, is larger than zero by far. (11) specifies when V_3 equals to V_{tn}. Nevertheless, as V_3 no longer reaches below V_{tn} in the whole oscillation cycle when V_{in} is high, such moment will not make appearance.

Another explanation of the fading and vanishing of oscillation could be obtained with analysis from the view point of the hysteresis shown in Fig. 8(d). When the input voltage reaches above the actual upper bound (in Fig. 7), the hysteresis

still exists. However, the hysteresis cannot support oscillation because the upper-left half of the hysteresis no longer has a steep edge. Instead, this edge has a gradient that could hold the circuit staying static at the intersection of itself and the load curve. Yet, this description of disappearance of oscillation from this viewpoint is difficult to quantify.

IV. Summary and Future Works

In this paper, a complete description for the oscillation process of the NTC is proposed. The body effect of one of the transistors is proved to be an important factor that supports the transition of the circuit from one phase to the other back and forth. The other important factor, as is mentioned in lots of previous works, is whether the gate-to-source voltage of M_2 is above its threshold voltage, which directly indicates the actual phase that the circuit is in. With the description of the oscillation, quantified analysis of an NTC can be carried out taking physical meanings into consideration. This paper corrected an already-existing way to calculate the input voltage bounds. The explanation for the existence of the bounds is also addressed in this paper.

With the results of this paper, the function of every MOSFET in the NTC is clearer, which could give rise to a series of subsequent works:

First, since the principle of oscillation is clear, a more systematic designing method can be put forward for configuring the parameters of the NTC to meet special demands. This should be of great benefit if the NTC were to be placed into a large network system where its input and output ought to meet requirements of external devices. Such requirements involve, for example, meeting given oscillation amplitudes, rates, input voltage bounds, and so on. In other words, how the NTC encode information needs to be investigated. A related work on the earlier version of the NTC can be found in [15].

Moreover, the oscillation description shed light on how these MOSFETs collaborate with each other, which may offer heuristics to construct NTC with similar structure but more advanced devices like FinFET.

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