Hardware-accelerated edge detection for polarimetric synthetic aperture radar data

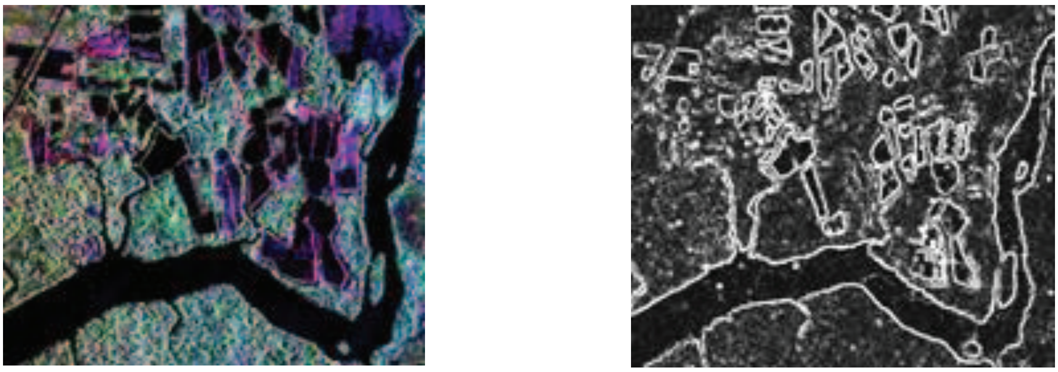
Quang Huy NGUYEN[1], Myo Tun AUNG[2], Ken Yoong LEE[2], Ian MCLOUGHLIN[1], Timo BRETSCHNEIDER[2]

[1]Nanyang Technological University
50 Nanyang Avenue, Singapore 639798
{nguyenquanghuy, mcloughlin}@ntu.edu.sg

[2]EADS Innovation Works Singapore
41 Science Park Road #01-30, Singapore 117610
{myo_tun.aung, ken-yoong.lee, timo.bretschneider}@eads.net

Abstract

Edge detection in polarimetric synthetic aperture radar (POLSAR) images is difficult due to the presence of speckle noise. In recent years, two constant false-alarm rate edge detectors were proposed for multi-look POLSAR data, namely the likelihood ratio edge detector [1] and the Roy's largest eigenvalue-based edge detector [2]. In the latter approach, the Roy's largest eigenvalue λ_{Roy}, which enables the identification of an edge, has to be computed. Given two independent complex Wishart matrices $\mathbf{Z}_{r1}$ and $\mathbf{Z}_{r2}$ of test regions $r1$ and $r2$ in an edge template, the following three main steps are performed to obtain the Roy's largest eigenvalue: (i) inversion of the two matrices $\mathbf{Z}_{r1}$, $\mathbf{Z}_{r2}$, (ii) computation of the complex multivariate matrices $\mathbf{Z}_{r1}\mathbf{Z}_{r2}^{-1}$ and $\mathbf{Z}_{r2}\mathbf{Z}_{r1}^{-1}$, and (iii) solving the determinantal equation $|\mathbf{Z}_{r1} - \lambda\mathbf{Z}_{r2}|=0$, which is identical to solving a cubic equation. An example result of a nine-look NASA/JPL POLSAR C-band data using the Roy's largest eigenvalue-based edge detector is shown in Figure 1.



(a) (b)

Figure 1: (a) Three-intensity NASA/JPL POLSAR image (HH, HV, and VV intensities are displayed in RGB), (b) edge detection result of (a) based on the Roy's largest eigenvalue.

Since the Roy's largest eigenvalue-based edge detector requires evaluation of a cubic equation, one major restriction is the computational speed of the original C-based implementation, whereby hardware acceleration is a requirement for remote sensing users to work interactively with geosciences applications, or for computation performed on-board a satellite or unmanned aerial vehicle (UAV). This paper describes a novel hardware-based edge detection architecture for POLSAR data based on the Roy's largest eigenvalue. The proposed architecture is capable of deriving edge-pixel images at a higher speed than its optimised software counterpart on an Intel Core2 CPU at 1.8GHz. The algorithm is implemented in a field-programmable gate array (FPGA) introducing an accelerated solution for POLSAR edge detection targeting acquisition data rates of up to 1 Gb/s.

One of the major challenges in performing this computation in a FPGA was the wide use of floating point (FP) computation (IEEE 754) in the software version. Full FP computation in hardware is infeasible due to resource requirements, and thus use of fixed point becomes necessary, with careful consideration of the maintenance of calculation accuracy. In particular, the Roy's largest eigenvalue is based on the computation of a cubic equation, which itself requires floating point operations for sine and cosine calculations. The proposed architecture thus approaches the cubic equation using a custom-tailored fixed/floating point evaluation module. As shown schematically in Figure 2, the resulting core architecture consists of four interlinked stages. In the first stage, edge templates with 7×7 pixels in size are used to compute the average covariance matrices for the two test regions. Then, these results are employed to produce the inverse matrix $\mathbf{Z}_{r1}^{-1}$ before the subsequent matrix multiplication $\mathbf{Z}_{r2}\mathbf{Z}_{r1}^{-1}$ in the third stage. High latency core devices are used in these stages for high frequency operation (100 MHz). Moreover, this enables a finer grained pipelined structure to be added and utilised during the waiting period, which improves significantly overall throughput. In the fourth stage, the cubic equation is computed through a chain of arithmetic computations, sine/cosine conversions as well as an arctan function to produce the final Roy's largest eigenvalue. On an Intel Core2 CPU at 1.80 GHz, the time needed to compute one pixel is 6.6 µs, while the computation requires only 1 µs on a FPGA (Xilinx Virtex-4, FX60). In order to reach 1Gb/s data transfer rate, multiple sections of the image are processed in parallel by multiple processors inside the FPGA.

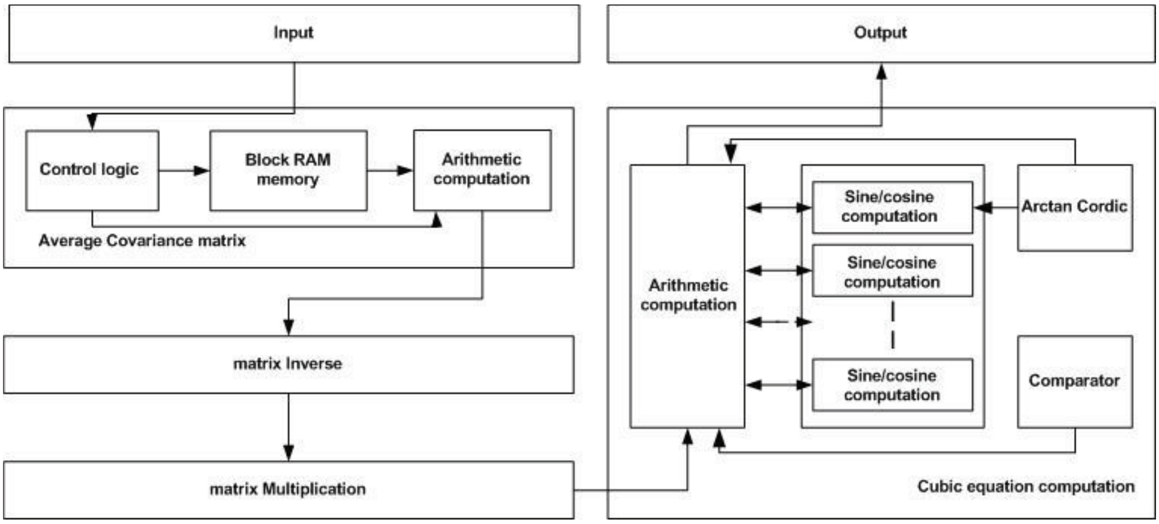


Figure 2: Block diagram for core computation of eigenvalue.

Conclusion

This paper has described a firmware implementation of an edge detection using the Roy's largest eigenvalue. An evaluation was carried out to assess that the solution performs comparable to a C language reference version, and yet improves significantly on the processing time experienced by a modern desktop PC. The implementation makes use of selected fixed-point calculations with scaling, arithmetic operations, and an arctan cordic function. The system is designed to be used to provide computation acceleration on PC, or to enable on-board processing of this technique on UAV or resource-constrained satellite computers.

References

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