ENHANCED DIGITAL UP/ DOWN FREQUENCY CONVERTERS

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Abstract:

Due to the increasing complexity in modern communication systems, State of the art data communication systems make extensive use of digital hardware. Besides baseband digital processing, the frequency tuning function is now being shifted from analog to digital implementation where the integration, cost, and case of programming are the primary motivations.

In this paper, a proposed technique for implementation of Digital Up Converter (DUC) and Digital Down Converter (DDC) is presented, avoiding the problem of bit growth in the Cascaded Integrator-Comb (CIC) filter which increases the bit error rate that affects the system performance due to the indeterminate data related growth in word length.

1. Introduction

In most communication systems DUC/DDC is the main process. The conversion process must support different wireless standards and bandwidths. An efficient way of performing decimation and interpolation was introduced by E. B. Hogenauer [1]. However in case of large rate changes, the proposed technique requires very narrow band filters, which is hard to be achieved. A modified CIC architecture improved the performance over the traditional CIC approach at very little extra cost [2]. In 1991, H. Samueli and T. Lin [3] had implemented a high-performance decimating digital filter using recirculating halfband filter architecture of high-order decimation/interpolation filter. Thereafter, programmable high-order decimation/interpolation filter is introduced [4].

This paper presents an alternative to the traditional digital frequency conversions architectures.

2. System Description:

The basic modules for DUC/DDC are the CIC filters [1], with the general transfer function given by:

$$H(z)=\left\{\frac{1-Z^{-R}}{R\left(1-Z^{-1}\right)}\right\}^{N} \qquad (1)$$

Where N is the number of stages, and R is the factor of interpolation or decimation. Alan, [2], succeeded to improve the passband and stopband of a symmetric nonrecursive filter by using multiple copies of the same filter that consumes more size in implementation, but it is restricted by factor R equals to 2^x, where x is an integer. The sharpened filter $H_{sharp(z)}$ is related to the original filter $H(z)$ by:

$$H_{sharp}(z)=H^{2}(z)\left[3-2H(z)\right] \qquad (2)$$

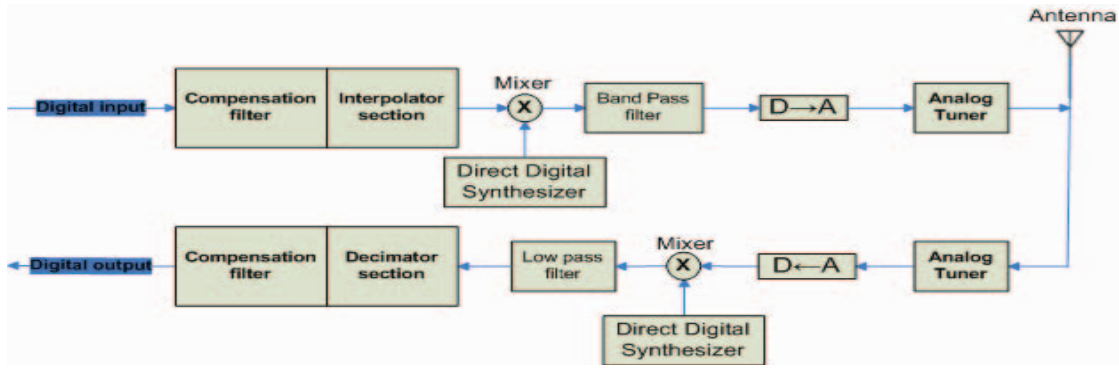
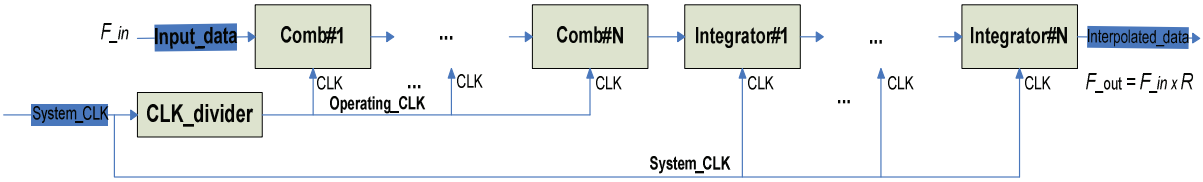


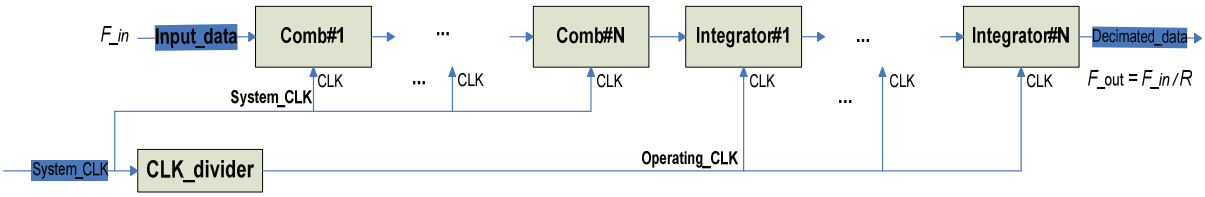
Fig. 1: The overall block diagram of the digital transceiver unit.

The above structures can be employed in digital transceivers as shown in Fig. 1. The interpolator section is required to separate the original baseband digital signal from its images, which is of a great benefit in reducing the required coefficients since sharp cutting edges for the stop frequency need huge filter coefficient also increase the size of the hardware implementation.

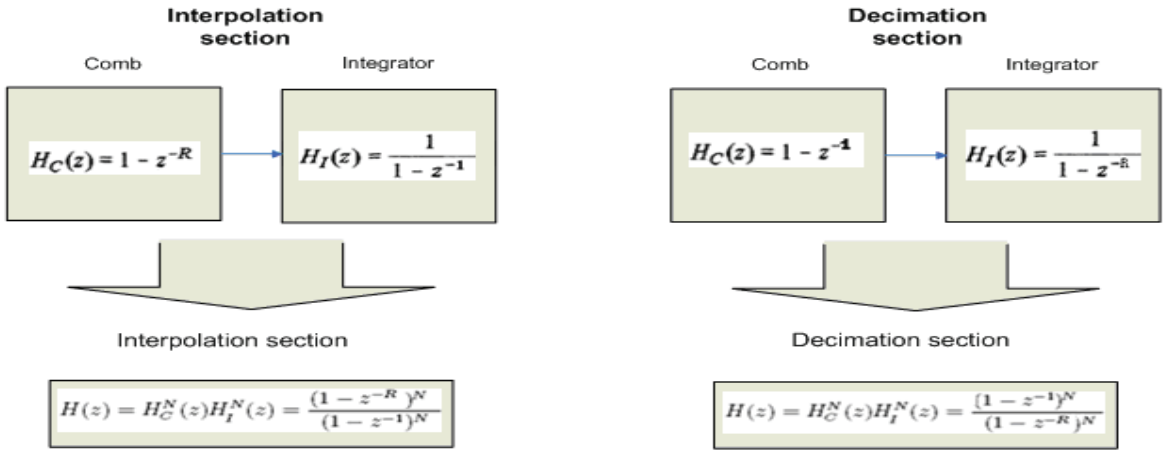
The proposed N-stages CIC filters for the interpolation and decimation process are shown in Fig. 2.



(a) Interpolation Section.



(b) Decimation Section.



(c) The general transfer function of the CIC filter.

Fig. 2: The proposed design; (a) Interpolation Section block diagram, (b) Decimation Section block diagram, and (c) The general transfer function of the CIC filter.

In Fig. 2, in case of interpolation, the sample rate is increased from *F_out/R* to *F_out* and again to *F_out/R* in case of decimation. Both the interpolation and decimation process are synchronized using two different clocks related by the used factor *R*. This approach avoids the use of the rate change switch.

The transfer function for a CIC filter is :

$$H(z) = H_I^N(z)H_C^N(z) = \frac{(1 - z^{-RM})^N}{(1 - z^{-1})^N} = \left(\sum_{k=0}^{RM-1} z^{-k}\right)^N \tag{3}$$

The differential delay (*M*) is a filter design parameter used to control the filter's frequency response, usually held to *M*= 1. The gain *G* at the output of the final integrator is:

$$G = (RM)^N \tag{4}$$

Then the output width (word length) is greater than the input width by:

$$\text{Max. path width} = i + \log_2\left((RM)^N\right) \tag{5}$$

Where, i is the word length of the input data.

3. Design and Implementation:

Consider a system with 10.7MHz *IF* frequency and narrow baseband signal of width 50KHz. Assume that the 10.7MHz output signal of the DDS is represented by 32 sample/period, so the sampling rate of the DDS output is 342.4M Samples/sec that give rise to the necessary interpolation factor R of 3420 in case of sampling the baseband at rate of 100K Samples/sec.

In the transmission section, as a result of the CIC interpolation process, the signal resolution before the mixer is 12-bit. Hence, the resolution of the DDS is selected to be 12-bit; that may enforce the implementation to employ an expensive D/A converter with 24-bit resolution. An alternative to this approach could be the gain reduction or rounding technique. However, both are considered a source of noise that reduces the overall performance. After the mixer, a simple bandpass filter of order 20 is designed using the FDA tool of MATLAB to remove the harmonics of the mixer. In the receiver section, a 12-bit A/D converter is selected to provide the same resolution of the DDS. An Equiripple lowpass FIR filter of order 20 is used to remove the harmonics of the mixing process before the decimation process. The bandpass filter has a worst case alias rejection of 75.86 dB, and the lowpass filter is of 78.92 dB. The design is tested on FPGA 4vfx12sf363-11 device on an evaluation board with 342 MHz clock frequency provided by built-in crystal oscillator.

4. Simulation Results:

The simulation results have been developed in two different platforms. The first is the MATLAB using the tools of the simulink, while the second is the Modelsim of Mentor Graphics using VHDL and Verilog developed codes for the proposed DUC and DDC. Using the simulink, Fig. 3.a shows a sine wave sampled base signal with a unity peak to peak. The interpolated output by a factor R = 3420 is shown in Fig. 3.b.

Obviously, the produced smooth sine wave reduces significantly the bandwidth of the sampled signal. While, the decimated one is shown in Fig. 3.c. Noting that the gain of the CIC exceeds 5e7 in 3 stages giving a rise to high amplitude of the interpolated signal. Also, the gain reduction may cause serious rounding and the original data retrieving becomes a difficult task. The simulation was also proved for a sampled base random signal.

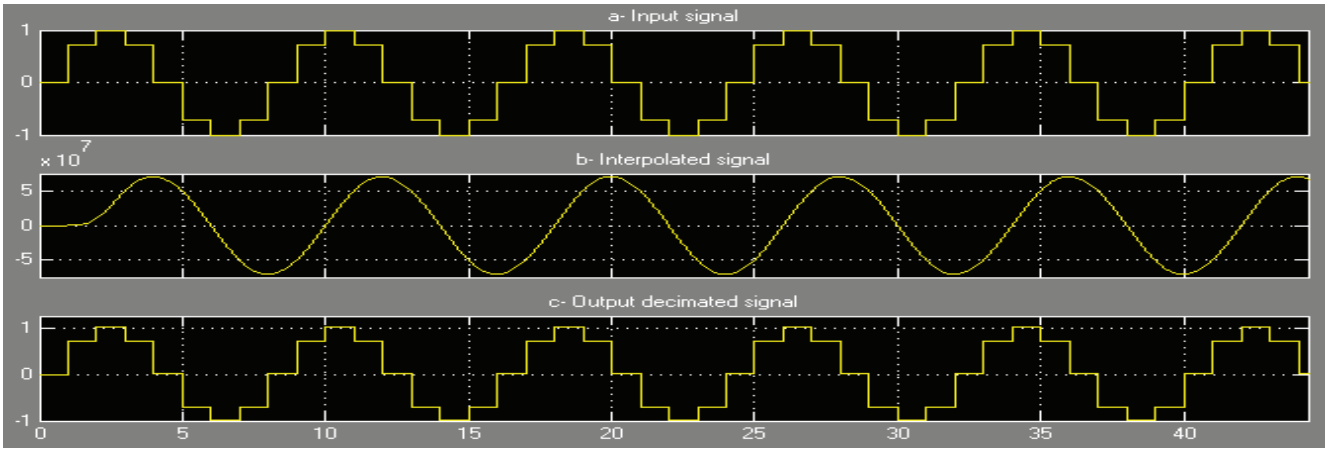


Fig. 3: the CIC simulation of sine wave sampled base signal; (a)Sine wave generator sample based signal, (b)The interpolated signal by factor R=3420, (c)The decimated signal.

The VHDL and Verilog developed codes are verified and tested using the Modelsim. Fig. 4 displays a random input signal, with a decimal radix, and the final decimated output. It can be noted that the output has been retrieved correctly after a delay interval measured by 6 operating_CLK. (one operating_CLK for each stage of the CIC interpolator and decimator).

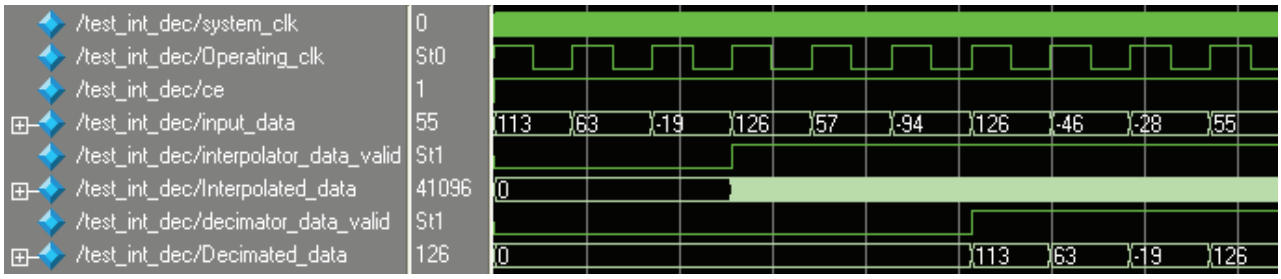


Fig. 4: The wave default simulation behavioral model of the input data, operating_clk, and output data.

5. Conclusion:

The proposed CIC interpolating and decimating filter architectures enable an efficient implementation of DUC and DDC for single-chip solution of digital communication system. This approach eliminates the need for the rate change switch that affects the size of implementation. Also the bit growth effect on the performance of CIC filter could be eliminated which achieves acceptable efficiency in design.

References:

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