THE DIGITAL WIDE BAND CHIRP PULSE GENERATOR AND PROCESSOR FOR PI-SAR2

Takashi Fujimura, Shingo Matsuo**, Isamu Oihara***, Hideharu Totsuka**** and Tsunekazu Kimura******

NEC Corporation (NEC), Guidance and Electro-Optics Division
Address : Nisshin-cho 1-10, Fuchu, Tokyo, 183-8501 Japan
Phone : +81-(0)42-333-1148 / FAX : +81-(0)42-333-1887
E-mail: * t-fujimura@da.jp.nec.com, ** s-matsuo@ax.jp.nec.com, *** i-oihara@ab.jp.nec.com, **** h-tozuka@pb.jp.nec.com, ***** t-kimura@df.jp.nec.com

BRIEF CONCLUSION

This paper shows the digital wide band chirp pulse generator and processor for Pi-SAR2, and the history of its development at NEC. This generator and processor can generate the 150, 300 or 500MHz bandwidth chirp pulse and process the same bandwidth video signal. The offset video method is applied for this component in order to achieve small phase error, instead of I/Q video method for the conventional SAR system. Pi-SAR2 realized 0.3m resolution with the 500 MHz bandwidth by this component.

ABSTRACT

NEC had developed the first Japanese airborne SAR, NEC-SAR for R&D in 1992 [1]. Its resolution was 5 m and this SAR generates 50 MHz bandwidth chirp pulse by the digital chirp generator. Based on this technology, we had developed many airborne SARs. For example, Pi-SAR (X-band) for CRL (now NICT) can observe the 1.5m resolution SAR image with the 100 MHz bandwidth [2][3]. And its chirp pulse generator and processor adopted I/Q video method and the sampling rate was 123.45MHz at each I/Q video channel of the processor.

After that, we had developed the experimental model of the digital wide band chirp pulse generator and processor for the airborne and spaceborne SAR in 2005. This model adopted the offset video method for the high performance, instead of the conventional I/Q video method. It had capabilities to generate the 300MHz bandwidth chirp pulse and to process video signals at 720MHz sampling rate for the input with 300MHz bandwidth. For the conventional signal generator by the I/Q video method, it is necessary to generate the In-phase(I) and Quadrature-phase(Q) signals and to mix two signals using an analog I/Q modulator. The frequency of output signal from the wide band chirp generator is much higher than that of the conventional narrow one. Therefore mutual timing condition should be strictly required for the generation of two signals (I and Q) and its mixing. Otherwise the phase error of I/Q modulation would be large. On the other hand, it is not necessary to mix I/Q signals for the chirp pulse generation with the offset video method. Therefore there is no phase error of I/Q modulation in this method. This is

why the offset video method for the digital chirp pulse generation is selected in order to achieve small phase error. The offset video method is also adopted for the signal processor by the similar reason. This method does not require strictly coherent sampling of two signals (I-ch and Q-ch) that is necessary for the I/Q video method.

Based on this wide bandwidth technology, we had developed the digital wide band chirp pulse generator and processor for Pi-SAR2 (for NICT) (see.Fig1). Its chirp generator generate can generate the 150, 300 or 500MHz bandwidth chip pulse on the offset video method. And its signal processor processes the video signal with the same bandwidth. This signal processor samples the offset video data at the frequency of 1.6 GHz and the quantization bit of 8bit. Then it demodulates the sampling data to the I/Q data and resamples this demodulated I/Q data at 200, 400 or 800 MHz by digital signal processing. The good performance as a SAR chirp generator and processor is confirmed by the loop-back chirp signal to signal processor including transmitter and receiver.

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Fig.1 The Digital Wide Band Chirp Pulse Generator and Processor for Pi-SAR2

Table.1 NEC's Chirp Pulse Generator and Processor

Parameter	for NEC-SAR	for Pi-SAR (X-band)	Experimental Model	for Pi-SAR2
Year	1992	1997	2005	2008
Customer of SAR System	for NEC R&D	CRL (now NICT)	for NEC R&D	NICT
Bandwidth	50 MHz max	100MHz max	300MHz max	500MHz max
Sampling Rate	63.5MHz	123.45MHz max	720MHz max	1.6GHz max
Sampling Bit	6bit max	8bit	8bit	8bit
Tx Chirp I/F	I/Q	I/Q	Offset Video	Offset Video
Rx Video I/F	I/Q	I/Q	Offset Video	Offset Video (Digital I/Q demod.)
Rx channel	2(I/Q) x 1ch (updated to 2 x 2ch)	2(I/Q) x 3ch	1ch	3ch
Data Recorder I/F Speed	32Mbps	512Mbps	no data recorder I/F	200Mbps x 3ch