The Effect of Gate Layout on Responsitivity of MOSFET THz Detector

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***Abstract*— In this paper an attention is paid to the existence of parasitic elements in a typical n-channel MOSFET devices that are often employed in sub-THz detectors and the role they play in when such devices are employed at sub-THz frequencies. An effective circuit model of such a structure was constructed. The most of the effort was put to investigate the influence of the layout of the MOSFET's Gate on the expected responsivity of the detector. In particular, attention was paid to the contacts between the metallization layer (MET) that connects the Gate to the outside world, and the polysilicon (POLY) layer that forms the actual Gate in a typical MOSFET.**

I. INTRODUCTION

A mass-produced imaging detectors working in the sub-THz frequency range were only possible after the sub-THz detection mechanism applicable also to the metal-oxide-semiconductor field-effect transistors (MOSFETs) has been reported in the literature in [1] and analyzed later in a number of papers dedicated to the underlying physics of the mechanism [2]-[4]. However, all the reported circuits based on MOSFETs seem to rely on a rough 1-dimensional model of the detection mechanism itself, which is difficult to employ in order to predict the effect of various technological parameters of MOSFETs on the responsivity of detectors built using the devices.

In this paper an attention is paid to the existence of parasitic elements in all typical n-channel MOSFET (n-MOSFET) devices that are often employed in sub-THz detectors and the role they play in the effective input impedance that should be expected from typical MOSFETs employed at sub-THz frequencies. An effective circuit model of the MOSFET is constructed, which is an extended version of a model shown in [5]. The model is used to obtain an improved estimation of the responsivity of a detector built of an antenna fabricated on a thinned-down substrate and monolithically integrated with a MOSFET. The most effort was put to investigate the influence of the layout of the Gate in a MOSFET. In particular, attention was paid to role of the contacts between the metalization layer (MET) connecting the Gate to the outside world, and the polysilicon (POLY) layer that forms the actual Gate in a typical MOSFET. The number of the MET-POLY contacts influences the in-series Gate resistance R_g and, depending on other parasitics present on the MOSFET structure, may adversely affect the responsivity of the detector to the sub-THz signals.

Additionally, the extended model accounts for parasitic capacitance between the POLY layer and the p-well ($c_{POLY\text{-}PW}$), the capacitance between the MET layer and the p-well ($c_{MET\text{-}PW}$) as well as capacitances formed by the POLY layers overlapping with the n^+-doped contact areas for Drain and the Source.

II. MODEL OF A MOSFET

A construction of a typical n-MOSFET gives rise to a number of effects that result in increased losses particularly when the device is subjected to signals of frequencies from the sub-THz range. A vertical cross-section through a transistor of this type is shown in Fig. 1a. together with lumped elements that represent the loss mechanisms spread over the structure. The ensuing effective circuit model of the structure is presented in Fig. 1b. with the channel replaced using the transmission-line theory with a impedance matrix Z_c given as:

$$Z_C = \begin{bmatrix} Z_0 \coth(\gamma_0 L) & Z_0 \tanh(\frac{\gamma_0 L}{2}) \\ Z_0 \tanh(\frac{\gamma_0 L}{2}) & 2Z_0 \tanh(\frac{\gamma_0 L}{2}) \end{bmatrix}, \quad (1a)$$

where

$$Z_0 = \sqrt{\frac{r_0}{j\omega c_0}}, \gamma_0 = \sqrt{r_o j\omega c_0}, r_0 = \frac{1}{n^{(2D)} e\mu W}, c_0 = \frac{\varepsilon_0 \varepsilon_r W}{d} \quad (1b)$$

with unit resistances r_0 and shunt capacitances c_0 of the channel, $n^{(2D)}$ being an effective 2-dimensional gate-bias

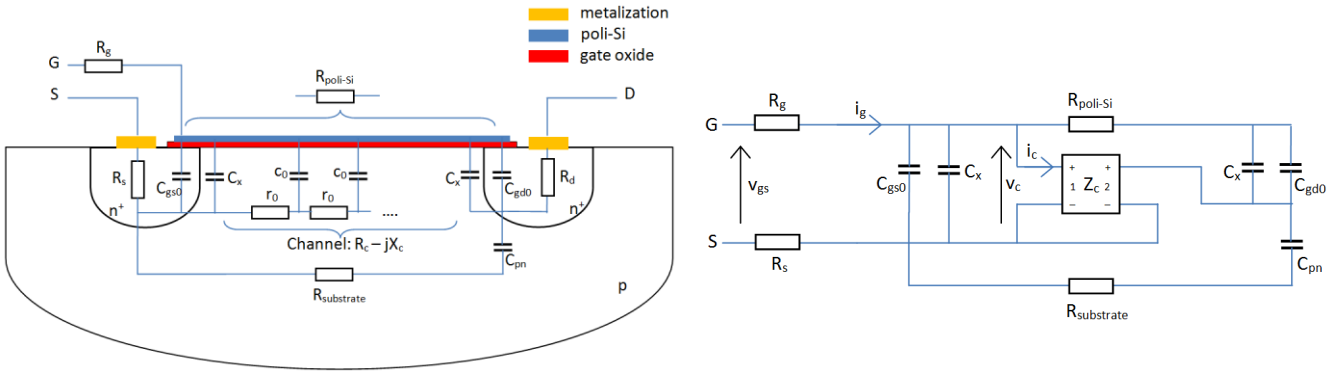

Fig. 1. a) A simplified view on a n-MOSFET fabricated on a p-type well with two ohmic contacts to Source and Drain and poly-silicon Gate on thin gate oxide shown together with basic mechanisms responsible for parasitic losses indicated and b) an effective circuit model of a typical MOSFET as seen through the G-S electrodes.

dependent carrier concentration in the channel, e is the elementary charge, μ is the carrier mobility in the channel, L and W are the channel length and width, and d is the thickness of the oxide layer, while ε_r is the relative permittivity of SiO_2.

A major loss mechanism – as explained in [5] – are the C_{gs0} and C_{gd0} capacitances that are linearly dependent on W. Their existence are a result of lateral diffusion of dopants in the contact areas n^+ under the gate oxide layer, which forms capacitors with metals plates separated only with extremely thin gate oxide. In reality, the structure is made more complex with an addition of a number of MET-POLY contacts. They may reduce N-fold (N being the number of contacts) the gate access resistance R_g.

However, at the same time they also increase the C_{gs0} capacitance by increasing the surface area of the POLY layer (the upper plate of an added capacitor) located over the p-well surface (the lower plate of that capacitor). As a result, the input capacitance C_{gs0} is defined as

$$C_{gs0} = C_{gs1} + C_{gs2} + C_{gs3} + C_{gs4}, \quad (2)$$

with

$$C_{gs1} = c_{gs0} \times W, \quad (3a)$$

$$C_{gs2} = c_{POLY\text{-}PW} \times A_c \times N, \quad (3b)$$

$$C_{gs3} = c_{POLY\text{-}PW} \times L_w \times L, \quad (3c)$$

$$C_{gs4} = c_{MET\text{-}PW} \times A_c \times (4 - N), \quad (3d)$$

where C_{gs1} is the gate overlap capacitance, C_{gs2} is a similar capacitance but formed by the POLY layer that surrounds each MET-POLY contact and is separated from the p-well by the oxide layer, C_{gs3} is a capacitance formed by the POLY track, while C_{gs4} is residual capacitance formed by the gate contact metallization layer (with surface area equal to ca. 4 contacts A_c) over the p-well. Thus, C_{gs4} falls as the number of MET-POLY contacts increase and the MET layer is effectively screened by the POLY layer of the C_{gs2} capacitance.

The parameter c_{gs0} is the unit parasitic capacitance dependent of the CMOS technology involved (after [5] it can be approximated as $1.4 \times W$), while $c_{POLY\text{-}PW}$, A_c and L_w are parameters defined for a given manufacturing process and describe, respectively, a unit capacitance between the POLY layer and the p-well surface, the minimum surface area of a single contact ($A_c = A \times A$), and the length of the distance between the contact and the edge of the gated region.

III. Results

The analysis involved structures of varying number of the MET-POLY contacts. Two such exemplary layouts are shown in Fig. 2a. The MET layer is show in dark blue, while the POLY layer is show in red and the MET-POLY contacts are shown in light gray. The modification of N, the surface area of the MET and the POLY layers as well as the channel area affect the parasitic resistances and capacitances present in the detecting structure. All these effects lead to a change in the amplitude of the THz signal voltage v_c. According to [2], the voltage is directly responsible for the photo-detection signal $\Delta U = e|v_c|^2 / (4k_BT)$, where k_B is the Boltzman constant and T is the temperature of the channel.

The performance of MOSFET-based detector can, thus, be analyzed by observing the behavior of $|v_c|$ as a function of N at a selected frequency of f = 335 GHz. Fig. 2b shows (normalized to maximum) the predicted amplitude $|v_c|^2$ in a structure excited trough the G-S pads with a signal of amplitude $|v_{gs}|$ = 1V.

The increase of the parasitic capacitances, which follows the growing number of the MET-POLY contacts, leads to estimated reduction of the $|v_c|$ by over 20%, despite the reduction of access resistance R_g. Thus, it seems that an effective way to increase the responsivity of detectors built using MOSFET devices is minimizing the area of their channel, even if this leads to a substantial reduction of the number of MET-POLY contacts and a slight increase of the R_g resistance.

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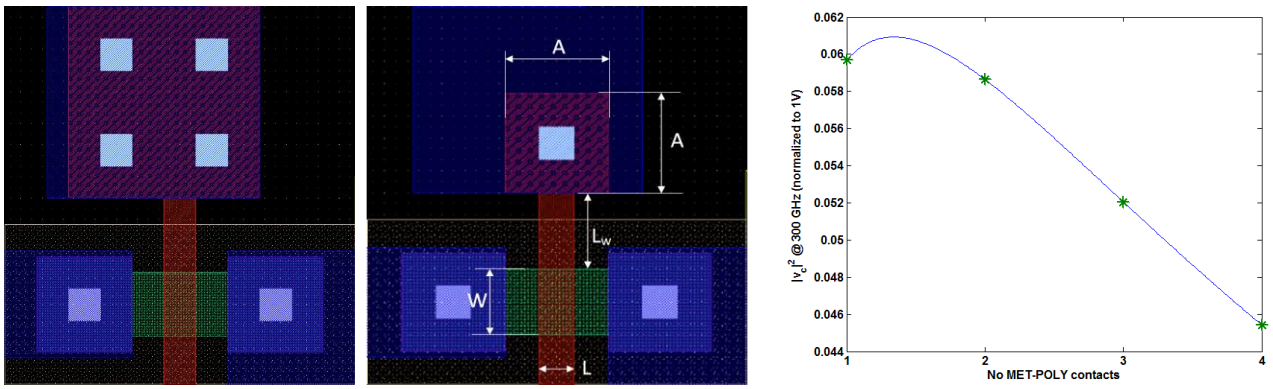

Fig. 2. a) The layouts of a MOSFET employing 4 or 1 contact between the Gate metallization layer and Gate poly-silicon layer and b) the channel voltage $|v_c|^2$ on an exemplary 6 µm × 3 µm MOSFET channel versus the number of MET-POLY contacts.