Compact Transmission Line Design in a Multi-Metallization Nano-CMOS Process for Millimeter-Wave Integrated Circuits

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***Abstract*—A compact transmission line design based on the conventional microwave stripline is presented for implementation of millimeter-wave CMOS integrated circuits. In a 65-nm process, the design gives a low insertion loss of 2.2 dB/mm at 60 GHz as determined by 3D electromagnetic (EM) simulations. A 50-Ω characteristic impedance is achieved resulting in a reflection coefficient of about -27 dB up to 80 GHz. The transmission line structure occupies minimal space of less than 17 µm in width and it accommodates active devices beneath it unaffected by any possible EM interference.**

I. Introduction

Millimeter-wave integrated circuits (ICs) in silicon CMOS technology has attracted much attention for the development of low-cost ultra-high data rate wireless communication systems operating especially in the 60-GHz unlicensed band [1]-[2]. In the realization of CMOS millimeter-wave ICs, the 90- or 65-nm technology nodes have been suggested as the best process option [2]. As transmission lines are important components in millimeter-wave ICs, it is worth investigating compact design of transmission lines in nano-CMOS processes, given that the commonly-adopted co-planar waveguide (CPW) design [3] occupies much IC area. In this work, a design based on the conventional microwave stripline is explored in a multi-metallization 65-nm CMOS process [4].

II. Transmission Line Structure in Nano-CMOS

Based on available process parameter data [4], physical values are first estimated (Table I) for the compact transmission line design. As shown in Fig. 1, the top five layers of metals are used for constructing the transmission line. In particular, the 12x thick metal form the signal-carrying core strip because the thickness is considerably larger than the skin depth (δ_{s60GHz} = 270 nm) at 60 GHz in copper. The core strip is surrounded by ground structure almost like a coaxial cable. However, an opening gap in the upper ground strip is made to allow the tuning of the transmission line's capacitance per unit length hence the characteristic impedance Z_0. A larger opening gap will reduce the capacitance between the signal-carrying core and the upper ground strip.

Table I. Process parameter data in the 8-level copper metallization 65-nm CMOS process and the estimated values used for the design of the 50-Ω compact transmission line

Test Parameter	Test Structure Data	Process Parameter	Estimated Value
M8 sheet resistance	7.73 mΩ/sq	M8 (copper) thickness	t_{M8} = 2.23 µm
M8-M7 capacitance	75 *a*F/ µm^2	ILD (SiO_2) thickness	t_{ox87} = 450 nm
M7 sheet resistance	6.27 mΩ/sq	M7 (copper) thickness	t_{M7} = 2.75 µm
M7-M6 capacitance	61 *a*F/ µm^2	ILD (SiO_2) thickness	t_{ox76} = 550 nm
M6 sheet resistance	40 mΩ/sq	M6 (copper) thickness	t_{M5} = 430 nm
M6-M5 capacitance	161 *a*F/ µm^2	ILD (SiO_2) thickness	t_{ox65} = 210 nm
M5 sheet resistance	87 mΩ/sq	M5 (copper) thickness	t_{M5} = 200 nm
M5-M4 capacitance	251 *a*F/ µm^2	ILD (low-*k*) thickness	t_{ox54} = 110 nm
M4 sheet resistance	87 mΩ/sq	M4 (copper) thickness	t_{M4} = 200 nm

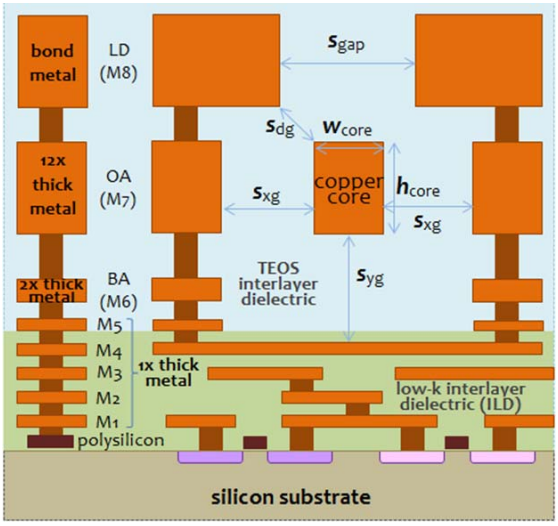

Fig. 1. Cross-sectional diagram showing the geometry of the proposed compact transmission line design in an 8-level copper-metallization 65-nm CMOS process.

III. Electromagnetic Simulation

To evaluate the compact transmission line design for CMOS millimeter wave ICs, electromagnetic (EM) computation using the finite element method (FEM) was performed with the material properties set accordingly, i.e. $\sigma = 5.8\times10^7$ S/m for copper, ε_r = 3.8 for TEOS (tetraethyl orthosilicate) SiO_2, and ε_r = 2.8 for low-*k* interlayer dielectric (ILD). Fig. 2 shows the electric field (in white arrows) and the current density distribution (in colour scale). The computed EM fields are then used to determine the voltage and current signals from which the characteristic impedance Z_0 as well as the S-parameters are calculated [5]. A loss tangent value of 2×10^{-3} [6] and a value of 0.6 [7] for the imaginary part of the complex ε_r have been set respectively for the TEOS SiO_2 and

the low-*k* ILD in the EM simulations. This is to account for the possible signal loss at GHz frequencies and beyond.

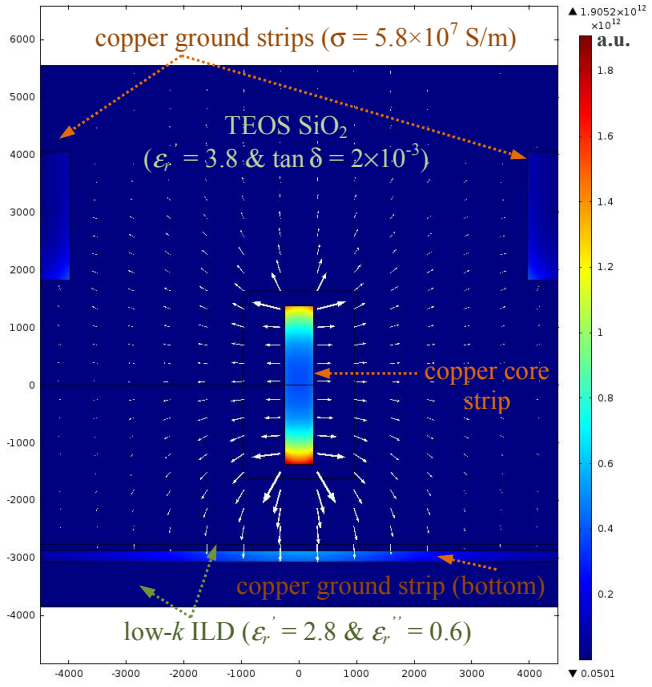

Fig. 2. Electric field (white arrows) and current density distribution (normal component) for a compact transmission line design with s_{gap} = 7.9 µm; the horizontal and vertical dimensions are in nm.

IV. Simulation Results

Fig. 3 shows Z_0 of the transmission line at 60 GHz for different gap sizes of the opening right above the signal-carrying core. It can be seen that $Z_0 \approx 50\ \Omega$ with a gap size of about 8 µm while keeping the imaginary part minimal. Fig. 4 shows the two-port S-parameter results from three-dimensional (3D) EM simulations run for the optimized 50-Ω stripline of 200 µm in length. The $|S_{11}|$ down to -27 dB confirms the successful 50-Ω design with a low loss of $|S_{21}|$ = -0.23 dB for a stripline of 200 µm long and 17 µm wide.

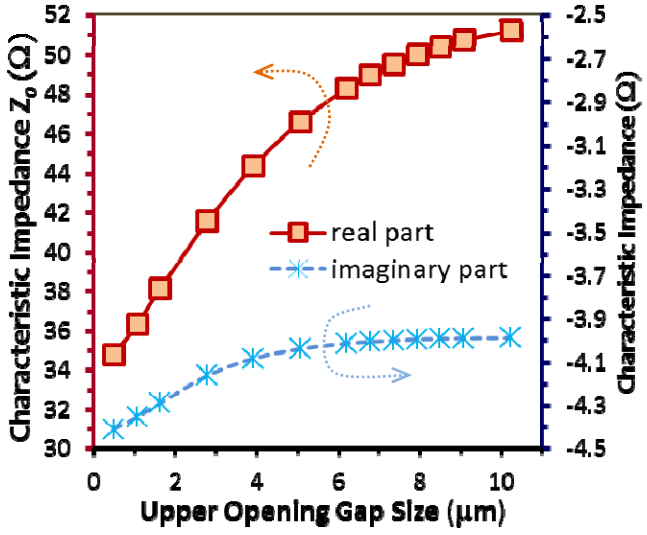

Fig. 3. Tuning of the characteristic impedance Z_0 of the compact transmission line by varying the gap size of the opening right above the core strip.

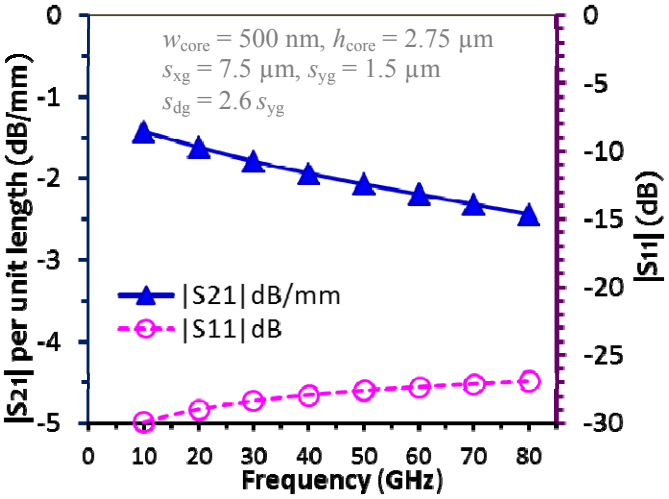

Fig. 4. Two-port S-parameter results from 3D EM simulation of the optimized 50-Ω transmission line with length = 200 µm and width < 17 µm.

V. Summary

A compact design of 50-Ω transmission lines in a 65-nm CMOS process has been reported. As determined by 3D EM simulation, the transmission line design based on the process test parameter data gives a low insertion loss of about 2.2 dB/mm at 60 GHz, with both the conductor loss and the dielectric loss already taken into consideration. The 50-Ω characteristic impedance results in a reflection coefficient of about -27 dB or better over a broad frequency range. Such a compact design of transmission lines is useful for implementation of millimeter-wave ICs in any other nano-CMOS processes with multi-metallization. Compared with the typical CPW design, the compact design presented in this work uses significantly less chip area apart from the advantage of eliminating high frequency substrate loss and crosstalk with surrounding interconnects and devices.

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