

A 0.6-1.2 THz Monolithic Imaging Array

Dan Corcos¹, Noam Kaminski¹, Danny Elad¹, Thomas Morf², Winnie Tatiana Silatsa Saha²,
Ute Drechsler², Lukas Kull², André Bischof³, Yingyun Zha³
¹IBM Research – Haifa, Haifa University Campus, Haifa, Israel
²IBM Research – Zurich, Säumerstrasse 4, Rüschlikon, Switzerland
³CSEM, Technoparkstrasse 1, Zurich, Switzerland

Abstract—A 19x8 pixel array with a read-out integrated circuit was designed and fabricated in a micro-machined SOI-CMOS process. The pixels are antenna-coupled MOSFET bolometers operating at room temperature in a wide 0.6-1.2 THz band. The read-out circuit features column multiplexed differential amplifiers, offset calibration capability and chopper stabilization.

We present the performance of the read-out circuit building blocks, as well as characterization results of the pixels, which demonstrate good detection sensitivity.

I. INTRODUCTION

THE successful realization of sensitive THz detectors in silicon technology is paving the way to large format focal plane arrays [1]–[2]. While room temperature bolometers demonstrated so far superior performance [3], additional processing steps are required for their fabrication. Accordingly, CMOS compatibility and process simplicity are very desirable for microbolometer arrays. A novel antenna-coupled bolometric detector was recently realized based on bulk micromachined SOI-CMOS dies [4]. Post-processing comprises few etching steps for achieving the required thermal insulation, whereas no additional layers are introduced.

The MOSFET bolometer design was used for implementing a 19x8 pixel array with column multiplexed analog read-out circuit. The pixels and the read-out integrated circuit (ROIC) are monolithically integrated on the same chip. A photograph of one chip is shown in Fig. 1 and the imager's architecture is shown in Fig. 2. The column amplifier has a gain of 53 dB and it supports chopper stabilization for removing its own $1/f$ noise from the signal bandwidth. A row of blind sensors is used for generating the reference voltage for the differential inputs. A 7 bit current steering DAC with 2.5 nA LSB allows removing the residual input offset.

II. RESULTS

We used a blackbody and a frequency multiplier chain for measuring the optical responsivity of the pixels with two complementary methods. These measurements were done in a test mode where the detector is directly accessible, independently from the ROIC. The post-processed pixels showed a responsivity of the order of 61 kV/W. The typical measured noise voltage spectral density (VSD) is $2.1 \mu\text{V}/\text{Hz}^{1/2}$ at 1 Hz with $1/f$ spectrum, which corresponds to a detector's NEP of $35 \text{ pW}/\text{Hz}^{1/2}$. The read-out circuit has a low input referred noise, of the order of $5 \mu\text{V}$ RMS, which drops to $1 \mu\text{V}$ if signal chopping is applied. While the detector and the (unchopped) read-out circuit generate by design approximately the same amount of noise, the pixel's noise rose to about twice that of the ROIC following the micro-machining process.

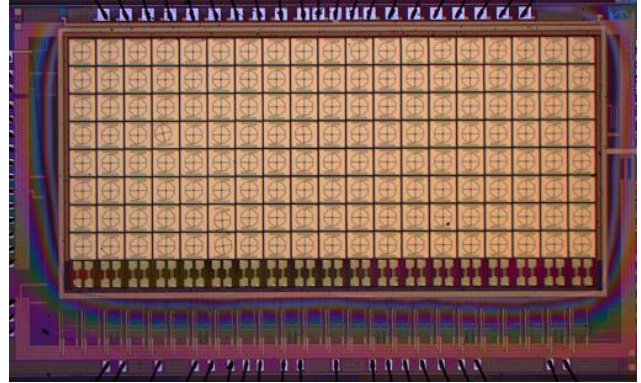


Fig. 1. Photograph of a 19x8 pixel array. The chip size is 7 mm x 3.3 mm.

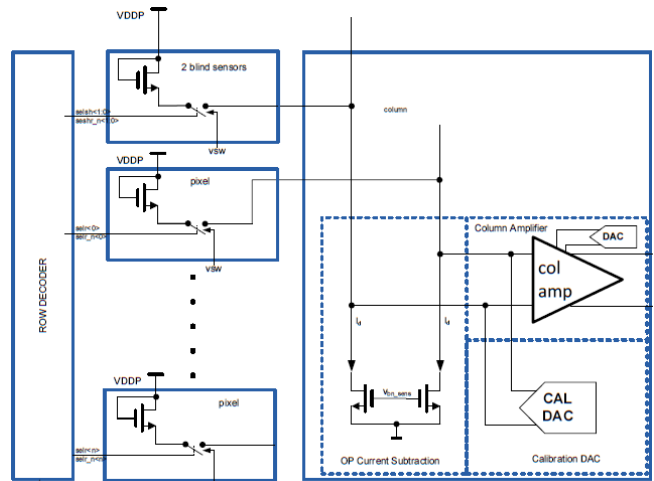


Fig. 2. Architecture of the read-out circuit front-end and pixel array.

The column amplifiers includes a 5-bit DAC for coarse offset cancellation. The measured DAC range is 5 mV (168 $\mu\text{V}/\text{LSB}$), which is sufficient for cancelling the variance of the amplifier's offset voltage ($3\sigma = 3 \text{ mV}$).

The total detection sensitivity of the sensor read through the on-chip electronics is expected not to change significantly since the detector's noise is dominant.

REFERENCES

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