Room-Temperature Remote Sensing: Far-Infrared Imaging based on Thermopile Technology

Giacomo Mariani, Matthew Kenyon
Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA, 91109 USA

***Abstract*— This work presents recent advances on room-temperature far-infrared thermopile detectors. The focal plane arrays micromachined at JPL are integrated with dedicated radiation-hardened read-out circuit chips to provide remote sensing under high radiation conditions environments.**

I. Introduction

THERMAL imaging is a remote-sensing technique capable of providing surface and atmospheric maps with high radiometric and spectral accuracy. Thermal imagers (TIs) based on thermopile technology are broadband, exhibiting a flat response over a wide spectral range (0.2-200μm), lightweight because no cryogenic cooler is required, and versatile as the detectors are insensitive to substrate temperature variations. This class of instruments has successfully flown on many missions such as Pioneer 10 & 11 (Infrared Radiometer), Voyager (IRIS instrument), Viking Orbiter (IRTM), Cassini (CIRS), Mars Reconnaissance Orbiter (MCS), and Lunar Reconnaissance Orbiter (Diviner) [1]. Thermopile pixels [2] are inherently insensitive to instrument temperature drifts, and highly linear to incident radiation with overall detector sensitivity $D^*>10^9$ cmHz$^{1/2}$/W @ 300K. For space mission, this work will focus on the current development of detectors able to tolerate harsh radiation environments [3] (e.g. Jupiter's magnetosphere) to understand geology and habitability, while providing vital reconnaissance for future landed missions.

II. Micromachining of Thermopile Arrays

When IR radiation impinges onto the imager, each thermopile pixel transduces the resulting pixel-to-substrate temperature difference into a voltage via Seebeck effect. *Figure 1* shows a close-up micrograph picture of one pixel in a thermopile array.

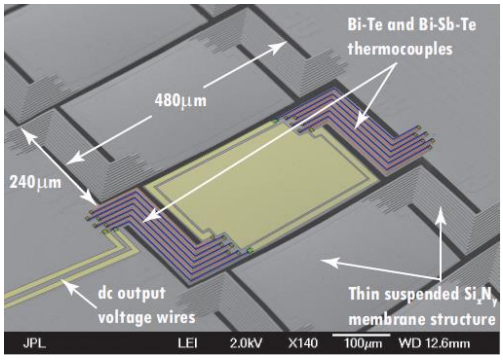

Figure 1: SEM micrograph of a segment of a 1-D detector array.

The thermopile detector arrays are fabricated utilizing well-established bulk micromachining techniques developed at JPL [1]. The thermopile arrays are built on commercially available silicon-on-insulator (SOI) wafers. SOI wafers have a buried oxide layer that we use as an etch stop when we remove the silicon from underneath the detectors. The first fabrication step is to deposit low-stress Si_xN_y that will constitute the final cantilevered/suspended membrane.

Next, metal contacts and thermoelectric couples are patterned using a lift-off technique. The thermoelectric materials are deposited by means of a load-locked customized co-evaporator which allows for quick turnaround while optimizing the composition of the n-type and p-type materials by adjusting the evaporation rate. Sputtering depositions would result into a device yield limited by lift-off process (edges of the photoresist stencil will be covered) as well as the preparation of numerous sputtering targets to achieve any stoichiometry optimization. Si_xN_y layer is then grown to protect and passivate the thermopile array.

Deep-trench reactive ion etching (DRIE) tool is used to remove the silicon from underneath the detectors. The etch stops on the oxide layer. The oxide layer is removed with buffered HF and then the wafer is diced into detector array chips. The final step is to use the XeF_2 tool to remove the remaining silicon from underneath the detectors. *Figure 2* shows an image of a typical micromachined thermopile array.

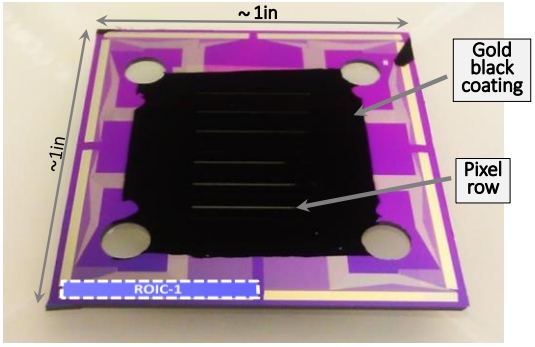

Figure 2: Fully-fabricated thermopile-based focal plane array.

III. Integration With Read-Out Chips

Following the focal plane array fabrication, each pixel output is connected to one input channel of the readout integrated circuit and the signal is modulated at high-frequency to avoid 1/f noise then amplified. JPL collaborated with Black

Forest Engineering (BFE) to design and build readout integrated circuits (ROICs) for the thermopile arrays. JPL and BFE developed a ROIC that incorporates the following properties of thermopile detectors: (i) their response is DC, (ii) their noise is dominated by their Johnson noise and (iii) their 1/f noise is neglible. The ideal readout, therefore, has no 1/f noise and a low noise figure (i.e. the readout noise is much smaller than the detector's Johnson noise.) To achieve this result, BFE designed a circuit where each pixel of the CMOS readout design has a chopper-stabilized amplifier. The input stage takes the DC signal from the detector and chops at the chopping frequency (KHz) where the 1/f noise of the amplifier is low. After amplification, demodulation, and integration at the pixel level, the signals are multiplexed to a single analog output stream. After amplification, the signal is demodulated back to base-band, digitized, and time-multiplexed at the output of the readout chip.

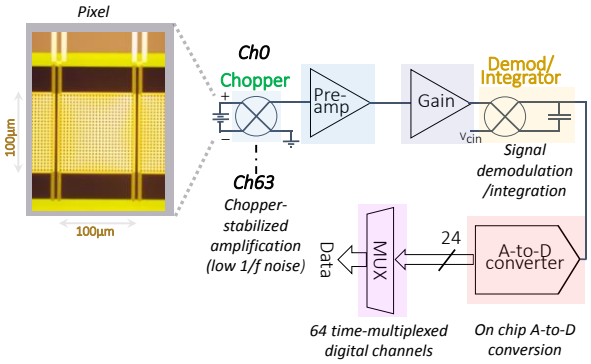

Figure 3: Complete signal chain of the thermal imager with digital output.

The complete schematic of the signal chain from pixel to data output is shown in *Figure 3*. Noise characterization reveals a total system noise of 77 nV/√Hz for a 120KΩ resistive load. High radiation levels (e.g. Jupiter's belt) set stringent requirements on radiation-hardened thermopile arrays [2] and read-out electronics that must operate under high-energy radiation and ions. Radiation-hardened by design (RHBD) is required to operate under high radiation conditions [3]. In RHBD approaches, the transistor topology is changed to annular layout, avoiding current leakage along the transistor edges. Preliminary total-ionizing dose measurements show that all the nominal values of power supply vary less than 2% from 0 to 3Mrad (Europa requirement). Five channels are tested, showing a remarkable high stability over time during radiation exposure.

IV. Focal Plane Assembly

The detector array and readout chips are mounted on an aluminum nitride hybrid substrate (see dashed white box and inset). The hybrid substrate is mounted onto a focal-plane block made of molybdenum. In *Figure 4* below, two chips are mounted onto the hybrid substrate. The figure is showing an example of MCS/Diviner focal plane assembly.

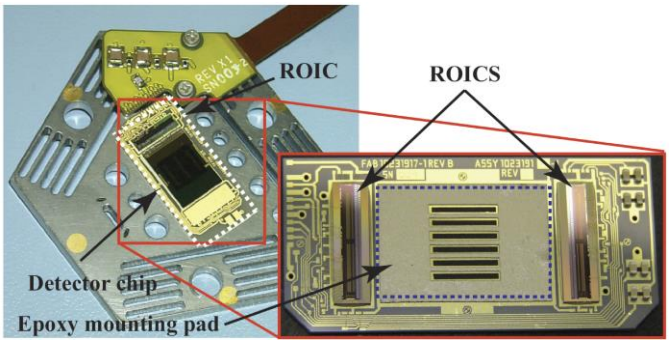

Figure 4: An MCS/Diviner focal plane assembly.

V. Summary

Fabrication of thermopile detector arrays and integration with rad-hard read-out chips are developed and tested to achieve remote sensing thermal imagers suitable to high radiation environments.

VI. Acknowledgement

The research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

References

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[2] M. C. Foote, M. Kenyon et al. "Thermopile detector arrays for space science applications", International Workshop on Thermal Detectors for Space Based Planetary, Solar, and Earth Science Applications TDW 2003.
[3] S. Gaalema et al. "Radiation hardness by design for mixed signal infrared readout circuit applications", Proc. SPIE 7780, 2010.