0.2 THz Push-Push VCO with Low Power, Low Phase Noise and High Oscillation Efficiency in 65 nm CMOS

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***Abstract*—This work presents a push-push voltage controlled oscillator (VCO) working at 0.2 THz. In order to improve the generated harmonic output power and provide low phase noise, a modified cross-coupled technique is applied. It employs a pair of inductors between the gate and drain of the cross coupled transistors to increase the gate impedance for harmonic signal. Based on the simulation it is found that the required transistor size can be reduced to achieve high phase noise performance with the help of an appropriate value of gate inductor. Since smaller transistor been used, the DC power consumption of the designed VCO is reduced and the parasitic effect is minimized. For evaluation purpose, the VCO is designed and fabricated in 65 nm CMOS. The measured output power is -13.7 dBm, consuming 10 mA DC current under 1.2 V Power supply. It realizes a high THz generation efficiency of 3.5‰ with a compact area of 0.027mm^2.**

I. INTRODUCTION

TERAHERTZ research has drawn increasing attention recently due to its unique capabilities in detecting and possibly analyzing concealed objects [1]. However, source generation at THz frequency is a major challenge, especially using the semiconductor technology such as CMOS. With recent advances in silicon-based devices, a number of VCOs realizing THz signal generation have been reported [2]-[6]. As traditional cross coupled VCO are heavily loaded due to large parasitic from active and passive components, the above mentioned VCO has low output power. In order to realize a high output power, very large DC power is required, leading to low DC-to-RF conversion efficiency.

This work demonstrates a push-push VCO working at 0.2 THz (200 GHz). In order to generate high output power while reduce the DC power consumption, a small inductor is placed at the gate of the cross-coupled oscillator. It is not only helpful to boost the harmonic power, but also lead to the phase noise improvement. The working principle of this method is studied based on mathematical analysis and circuit simulation. For evaluation purpose, the designed VCO is fabricated in 65 nm CMOS technology. Measured results show that the proposed VCO achieves -13.7 dBm output power at 204 GHz with 10 mA DC current under 1.2 V power supply.

II. CIRCUIT DESIGN AND ANALYSIS

Generally, in order to produce higher output power, transistors with large size are preferred. However, this will result a higher DC power consumption, leading to a poor DC-to-RF transfer efficiency. Large transistor will also limit the maximum achieved oscillating frequency due to higher parasitic at THz frequency. To cope with the contradiction problems, Fig. 1 gives the proposed VCO with a very simple structure. Cross-coupled LC topology is applied in this deign due to its simple structure and robust operation characteristic.

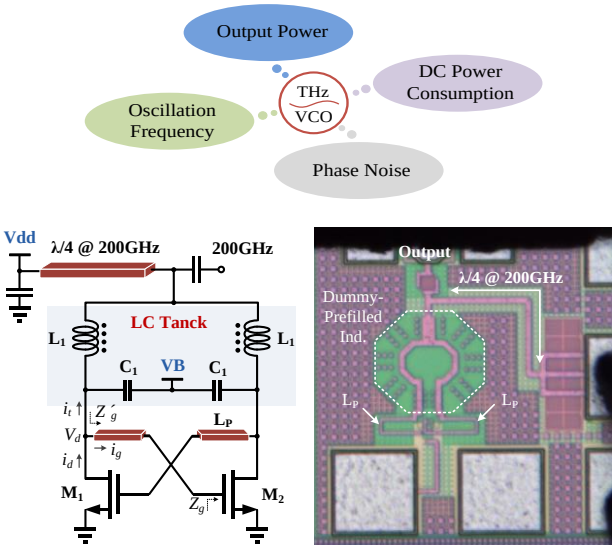


Fig.1. Schematic and chip micrograph of proposed push-push VCO.

Since any active devices will introduce noise into the VCO tank and degrades the phase noise performance, therefore, the widely used tail current is not employed in this design. The VCO oscillating at a fundamental frequency of 102 GHz, the second harmonic of 204 GHz is extracted from the virtual ground node using a quarter wavelength transmission line (0.2 THz). The inductor L_P between the gate and drain of the cross coupled pair will increase the load quality factor of the LC tank, in this way, the active device size can be reduced. As a result, the DC power consumption will be reduced. This can also been considered as an efficiency improvement of g_m generation as a smaller transistor size is used, leading to the performance improvement of phase noise [7].

The harmonic enhancement of the designed VCO can be comprehended through the boosted harmonic current into the LC tank [6]. The harmonic current generated at the drain of M_1 is separated into two paths: one of which flows into the LC tank with value of i_t and another part returns to the gate of transistor M_2 with current value of i_g. i_g can be defined by the drain voltage of M_1 and the gate impedance of M_2 as

$$i_g = \frac{V_d}{j2\omega L_P + Z_g}$$

Since L_P gives gate impedance enhancement, therefore, the harmonic current enter into M_2 is minimized. This not only help to increase the harmonic current into the LC tank, but also alleviates the mixing effect in transistor M_2, which in turn helps to produce higher harmonic output. However, with the variation of L_P value, the fundamental voltage landed on the gate of M2 also varies, which means the effect of the inductor value of LP should be overall considered. For better understanding of the

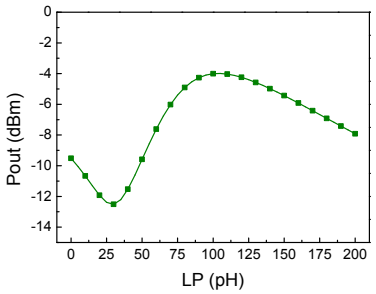
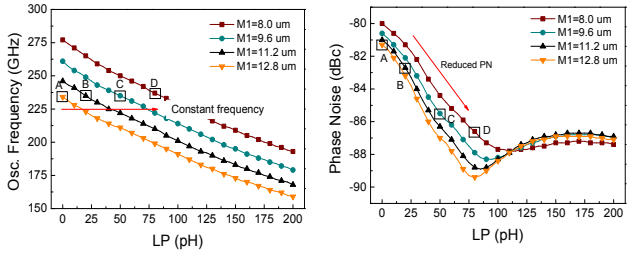


Fig.2. Simulated output power versus LP values.



(a) (b)

Fig.3. Simulated oscillation frequency and phase noise versus L_P values with different transistor size.

enhancement of harmonic generation, Fig.2 depicts the output power versus the increase of inductor value of L_P. As has been indicated, the output power varies with different L_P values. There is a maximum output power with an optimum inductor as shown in Fig. 2.

The effect of L_P value to the oscillation frequency and phase noise is studied in Fig.3 with different transistor size. From the simulated results it can be seen that large transistor size will help to reduce the phase noise at certain circumstance due to an increased transconductance of g_m. However, the achieved operation frequency will decrease if large transistor been used. With the help of LP, transistor with small size can be used while the phase noise will be improved.

III. Measured Results

The circuit and chip micrograph is given in Fig. 1, where the core area occupies 180 x 150 µm. To deal with the dummy density process, a dummy-prefilled center-tapped inductor is used. The length of the transmission is optimized so that it can resonate out the parasitic capacitances coming from the RF pad and other interconnections. The designed VCO is fabricated in TSMC 65 nm CMOS. Fig.4 shows the measurement setup and the measured output spectrum using external down-converted mixer. The circuit consumes 10 mA DC current from 1.2 V supply. The conversion loss of the measurement setup is around -71 including down-conversion mixer (-65 dB), RF probe and cables (6 dB). Due to immense setup losses at THz frequency, it is unable to directly obtain the phase noise through experiment. Using EM simulation tools, it is found that there is 5 dB phase noise improvement compared with conventional cross coupled VCO. Table I summarizes the performance of designed VCO and its comparison with the reported works. Due to the adoption of harmonic power boosting inductor at the gate of cross-coupled pair, the designed VCO owns the highest oscillation efficiency while a compact chip area is realized.

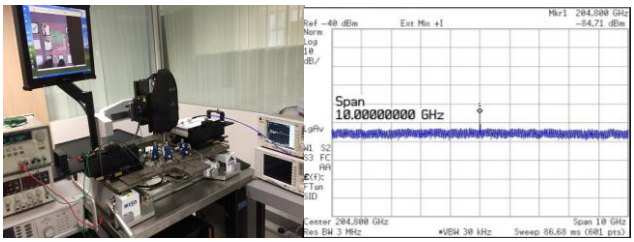


Fig.4. Measurement setup and measured output spectrum.

Table I Comparisons of 0.2 THz CMOS VCO

Freq. (THz)	P_{out} (dBm)	P_{DC} (mW)	Area (mm^2)	Eff. (‰)	Ref.
0.257	-17	71	0.052	0.08	[3] JSSC
0.288	-1.5	275	0.018	2.6	[5] JSSC
0.290	-1.2	325	0.36	2.3	[6] JSSC
0.204	-13.7	12	0.027	3.5	This work

IV. Summary

A push-push VCO is designed and measured. In order to improve the generated harmonic power, a pair of inductors are employed into the gate of the cross coupled pair to increase the gate impedance for harmonic signal. With the help of gate inductor, the output power and phase noise of the VCO is improved. Since smaller transistor been used, the DC power consumption is reduced. The measurement shows the highest oscillation efficiency compared with the state of the art 0.2 THz CMOS signal sources.

V. Acknowledgement

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