BiCMOS Integrated Waveguide Power Combiner at Submillimeter-Wave Frequencies

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***Abstract*—This contribution presents the development of an integrated power combiner in Bi-CMOS technology employing artificial dielectric layers (ADLs) at submillimeter wave frequencies. The power is gathered from frequency multiplier chains into a single waveguide which is loaded with ADL in order to reduce the structure footprint.**

I. INTRODUCTION

BI-CMOS technology recent advances [1, 2] have allowed the development of integrated heterodyne generators and receivers in the sub-millimeter band for communications, sensing and imaging applications. However, sub-mmwave system realized in this technology are still hampered by the limited power available due to the f_T/f_{max} and parasitic loading to the active device. Hence, compact and low loss power combiners are required to increase the output power delivered from the active devices.

Conventional microstrip line combiners exhibit high losses and require large area consumption at millimeter-waves [3, 4]. For instance, the already compact 8:1 Wilkinson combiner, presented in [4] requires an area of circa 0.1 x 1mm^2.

In this contribution a new structure, fully compatible with integrated technology fabrication rules and requirements, improving the compactness of power combining with tolerable losses over larger bandwidths, is presented.

II. WAVEGUIDE POWER COMBINER

The proposed power combiner concept, designed at 300 GHz, gathers the power from different integrated active frequency multiplier chains into a single waveguide as shown in Figure 1. The integrated active components are designed and integrated below the waveguide level to make the structure compact. Based on the available drive power and harmonic-balance simulations of the doubler circuit, an output power larger than -3 dBm can be obtained with an 8 dBm drive signal. The waveguide cutoff frequency will filter the 150 GHz spurious harmonic generated by the doubler.

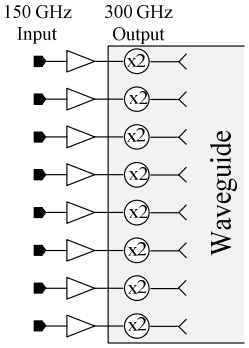

Figure 1. Simplified schematic of the power combiner structure.

From each frequency multiplier chain, a pin goes from the output pad of the SiGe HBT transistor collector to the input of the waveguide. The feeding pins are equally spaced within the waveguide as it is shown in Figure 2, and excite the fundamental TE_{01} mode. The waveguide is integrated within the BiCMOS wafer using Metal 2 and the top metal layer AlCap, see Figure 3. Metal 1 layer is left free for the circuit implementation. Thus, the maximum height of the waveguide is around 9.5 um. The walls of the waveguide are implemented using metal vias pins that go from metal 2 to AlCap layer, as shown in Figure 2, and provide a good confinement of the field inside the structure.

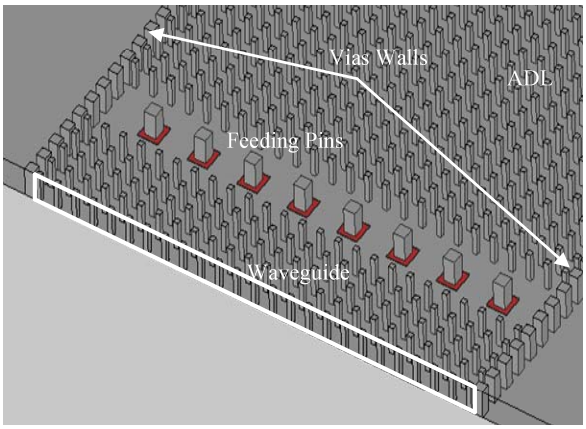

Figure 2. Structure of the power combiner waveguide end.

An artificial dielectric layer (ADL) [5 - 7] allows to enhance the permittivity of the substrate, in this case SiO_2 which has a relative permittivity of $\varepsilon_r = 4$. The ADL layer is implemented by the use of metal pins going from Metal 3 to Metal 6 in the BiCMOS stratification (see Figure 3), leaving a small gap top and bottom of the pin to the waveguide walls. The electric field is confined within this gap creating a capacitive effect which provides a slow-wave propagation; and thus, the substrate behaves as dielectric with higher permittivity.

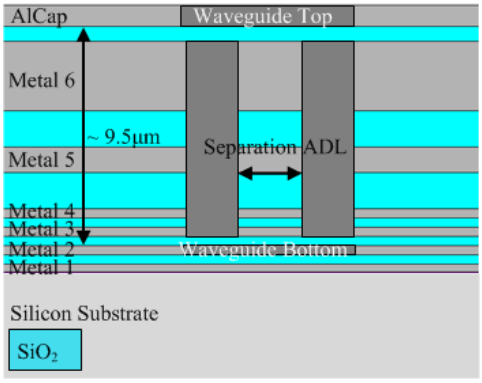

Figure 3. Metal stack of the BiCMOS technology wafer.

The enhancement of the permittivity can be controlled by varying the distance between the ADL pins as shown in Fig. 2 (Right). The maximum (effective) permittivity that can be achieved with the current BiCMOS technology is around 15. The higher the enhancement the more compact the structure becomes, it reduces both, the transversal and longitudinal dimensions of the waveguide. However, the finite conductivity of the metal in this structure adds up to 2.5dB/λ_g of Ohmic losses. Therefore, there is a tradeoff between the losses and compactness of the structure achieved.

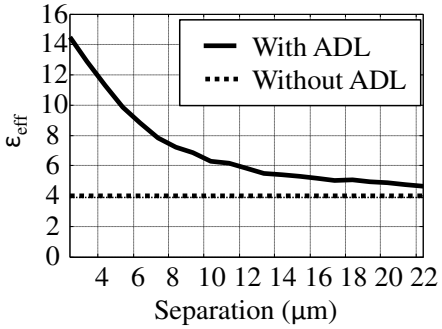

Figure 4. Effective permittivity as a function of the ADL pin separation.

In this contribution we will show the design and implementation of both: the electric circuit and the waveguide structure, as well as their tradeoffs and challenges.

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