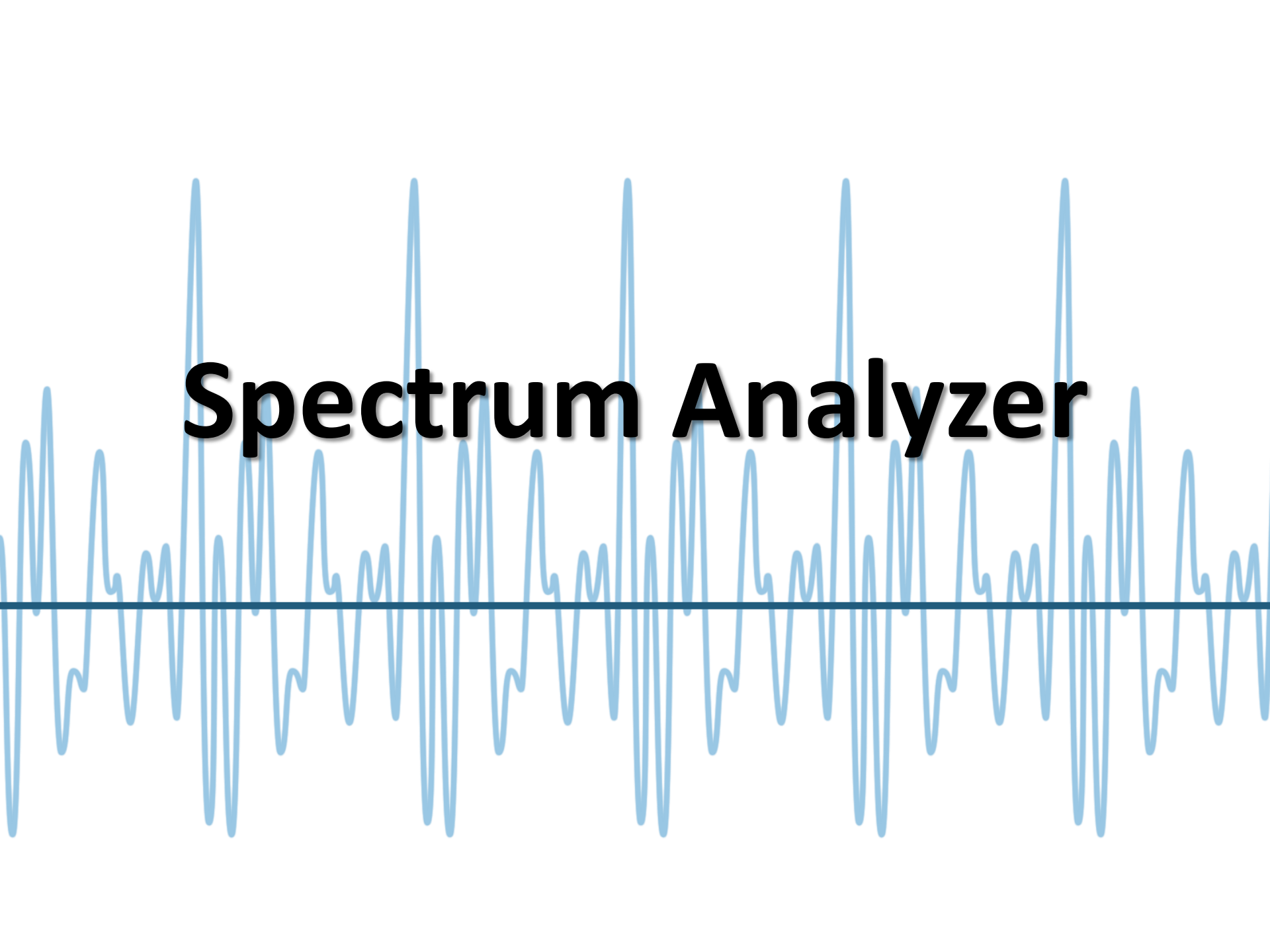


A blue waveform, resembling a spectrum or a signal, is plotted against a white background. The waveform consists of multiple peaks and valleys of varying heights and widths. A solid horizontal blue line runs across the middle of the image, serving as a baseline for the waveform.

Spectrum Analyzer



Introduction

Spectrum - Frequency range of waves

Analyze - subject to an analysis

Applications:

- Measure spectral purity of multiplex signals
- Measure Modulation Characteristics of AM, FM
- Measuring Frequency Response of Devices

**** Measure Audio Spectrum ****

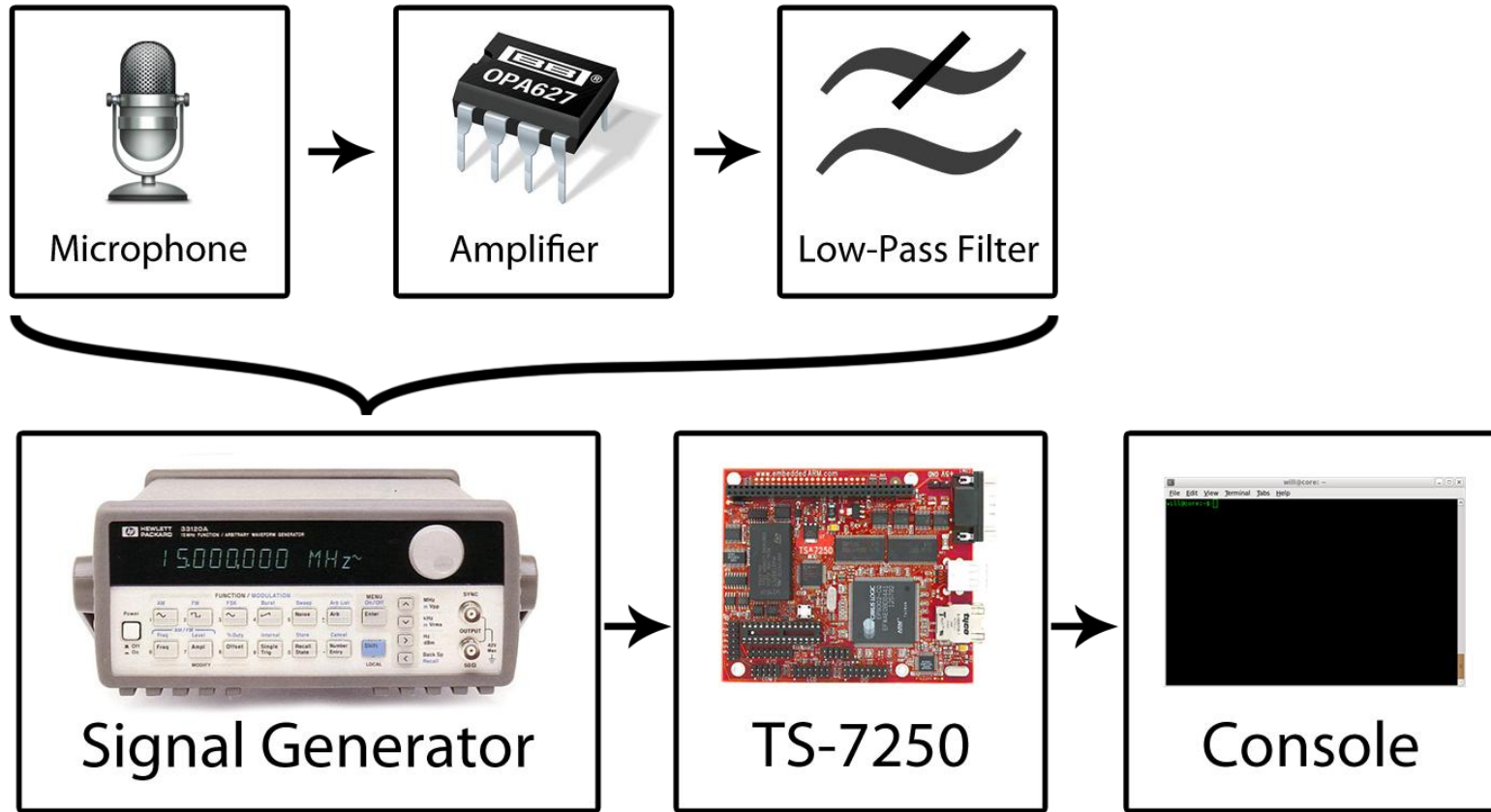


Introduction (Cont'd)

Topics Applied From Class:

- Dynamic Memory Allocation
- Pthreads
- Real Time Tasks
- Consumer / Producer Model
- Round Robin Scheduling
- Semaphores

Hardware Diagram





Design (Sampling)

Freq Range: (100Hz – 22kHz)

Sample Rate: $2 * f_{\max} = 44.1\text{kHz} = \text{CD Quality}$

Min Samples: $2 \left(\frac{T_{\max}}{T_{\min}} \right) = 2 \left(\frac{\frac{1}{100}}{\frac{1}{44100}} \right) = 441 \approx 512$

Expected Time: $512 \left(\frac{1}{44100} \right) = 0.0116 \text{ sec}$



Design (FFT)

FFT requires factor of 2^N inputs (64,128,256,512,etc..)

Complexity: $M \log M$, $M = 2^N$, $2^N \log 2^N = N 2^N \log 2$

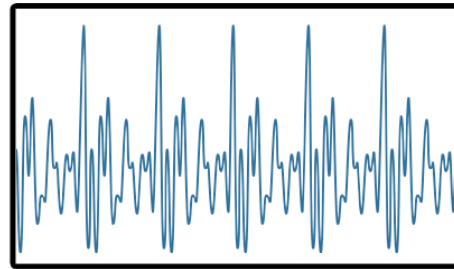
Symmetric Output, Discard Negative Frequencies



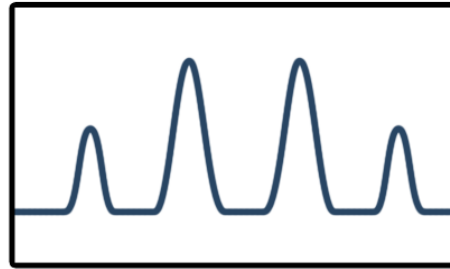
Design (Display)

- Problem: No VGA controller
- Solution:
 - Output 2D Matrix to create bar graph
- Frequency increase linearly to the right.

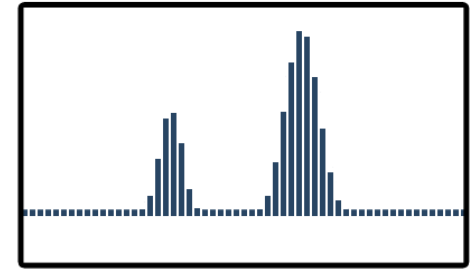
Software Diagram / UML



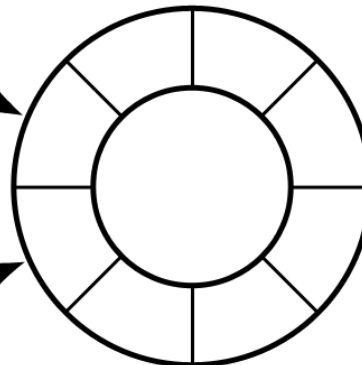
Task 1 - getSamples()



Task 2 - computeFft()



Task 3 - displayData()



Ring Buffer

Goal: User does not notice lag in system: 0.3sec



Closer Look at Ring Buffer

Offset	Data Type	
+0x00	enum status:	OPEN, LOCKED
+0x04	enum stage:	OVERWRITE, RAW_DATA, FFT_DATA
+0x08	double vReal[512]:	0
+0x10		1
...		...
		511
	double vImag[512]:	0
		1
		...
		511



Real Time Constraint

- DAC
 - Analog to Digital Conversion (ADC) via the onboard MAX 197 chip (MIN: 12 μ S)
 - Periodic Real Time Tasks to ensure consistent sampling of signal



C/P Model - RR Scheduling

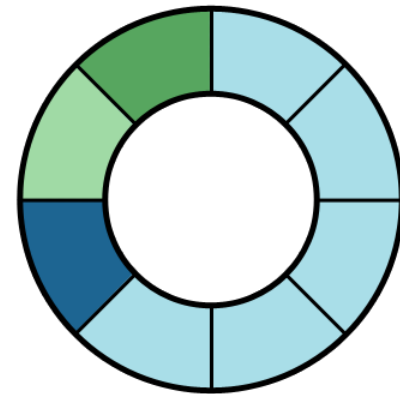
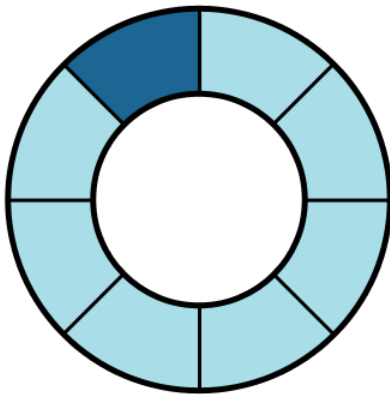
- Each of the threads has different execution time
- With Priority / Time slice RR: FFT thread and Display thread can be processing on another buffer while waiting for DAC conversion



Semaphores

- Use Counting Semaphores to Denote Available Resources
- `get_samples()` semaphore is initialized to the total number of buffers in the ring (10)
- Each thread signals the semaphore for the next thread.

Visual Buffer/Semaphores



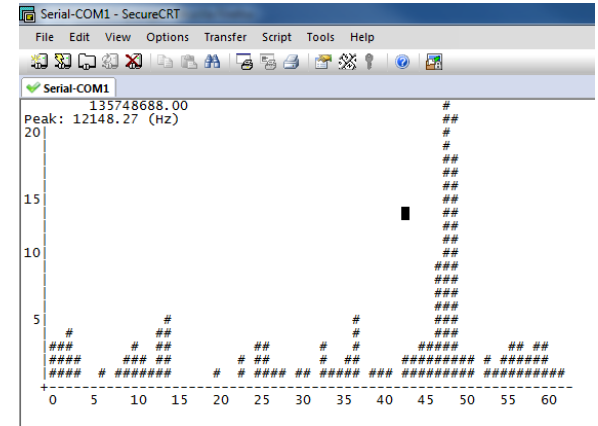
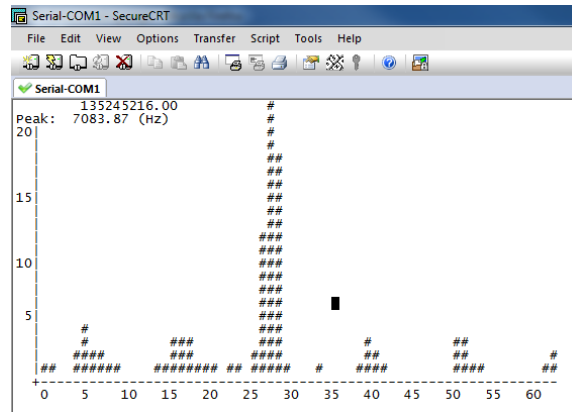
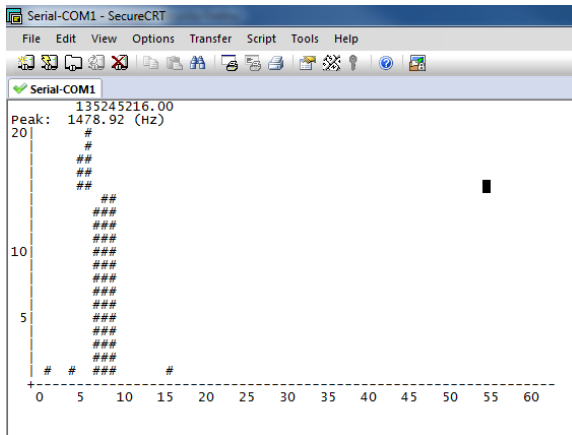


Results

Samples	Avg. Delay (ns)
64	75.87
128	158.23
256	N/A
512	N/A
1024	N/A
2048	N/A

Input Frequency (Hz)	Measured Frequency (Hz)
1000	970 – 1005
2000	1970 – 2010
4000	3900 – 4050
6000	5900 – 6070
8000	5900 – 8050
10000	6700 – 10100
12000	7000 – 12100
14000	8000 – 14200

Results





Possible Improvements

- ** Fix Sample Limitation
- * Find Optimal Conversion Factor
- Be able to discard buffers that have old data
- Improve algorithm for finding next buffer
- Upgrade Graphical Display
- Build full DAC setup with breakout serial cable and Microphone



Questions

